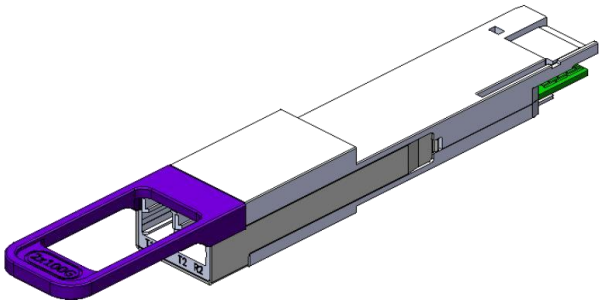
Single-Mode 2x100G QSFP-DD CWDM4 10km Transceiver

Features



- Supports 206Gbps
- Single 3.3V Power Supply
- Power dissipation < 8.0W
- up to 10km over SMF
- RoHS-6 compliant (lead-free)
- QSFP-DD MSA Compliant
- 8x25G electrical interface
- Dual CS connector
- Commercial case temperature range of 0°C to 70°C
- 8*25Gbps DFB-based CWDM transmitter
- PIN and TIA array on the receiver side
- I^2C interface with integrated Digital Diagnostic Monitoring
- Safety Certification: TUV/UL/FDA*Note*
- RoHS Compliant

Applications

- 2x100G QSFP-DD CWDM4 applications with FEC

Ordering Information

Part No.	Data Rate	Fiber	Distance *(note2)	Interface	Temp.	DDMI
DO-2QDCLR-10	206Gbps	SMF	10km	CS	0~+70℃	Yes

Product Description

The QSFP-DD transceiver module is designed for use in 200 Gigabit Ethernet links over 10km single mode fiber. The implementation of an 8 channel TOSA and ROSA to create a Dual CWDM4 transceiver. The 8 channel optical engines, which include dual embedded CWDM4 multiplexers. The 2x100G CWDM4 QSFP-DD transceiver is characterized by an 8x25G NRZ electrical interface and Dual CS connectors. And compliant with QSFP-DD MSA.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Operating Relative Humidity	RH	5	85	%
Receiver Damage Threshold, per Lane	Rxdmg	5.5		dBm

*Exceeding any one of these values may damage the device permanently.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	Tc	0	25	70	°C
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Power Dissipation	P_D			8	W
Instantaneous peak current	Icc_ip			3200	mA
Sustained peak current	Icc_sp			2640	mA
Steady state current	Icc			2308	mA

* Power Supply specifications, Instantaneous, sustained and steady state current compliant with QSFP-DD MSA Power Classification.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Transmitter						
Differential data input swing per lane				900	mv_{p-p}	
Input Impedance (Differential)	Zin			10	%	
Stressed input parameters						
Eye width		0.46			UI	
Applied pk-pk sinusoidal jitter		IEEE 802.3bm Table 88-13				
Eye height		95			mv	
DC common mode voltage		-350		2850	mv	
Receiver						
Differential output amplitude		200		900	mv_{p-p}	

Output Impedance (Differential)	Zout			10	%	
Output Rise/Fall Time	t_r/t_f	12			ps	20%~80%
Eye width		0.57			UI	
Eye height differential		228			mv	
Vertical eye closure				5.5	dB	

Parameter	Symbol	Min.	Typical	Max.	Unit
Transmitter					
Signaling Speed per Lane	BRAVE		25.78		Gbps
Data Rate Variation		-100		+100	ppm
Lane_0/4 Center Wavelength	λC0	1264.5		1277.5	nm
Lane_1/5 Center Wavelength	λC1	1284.5		1297.5	nm
Lane_2/6 Center Wavelength	λC2	1304.5		1317.5	nm
Lane_3/7 Center Wavelength	λC3	1324.5		1337.5	nm
Total Average Output Power	Po			8.5	dBm
Average Launch Power each Lane*(Note3)	Peach	-6.5		2.5	dBm
Transmit OMA each Lane *(Note4)	TxOMA	-4.0		2.5	dBm
Launch power in OMA minus TDP, each lane	OMA-TDP	-5.0			dBm
Transmitter and Dispersion Penalty per Lane *(Note5)	TDP			3	dB
Side Mode Suppression Ratio	SMSR	30			dB
Optical Return Loss Tolerance				20	dB
Transmitter Reflectance *(Note6)				-20	dB
Extinction Ratio	ER	3.5			dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}*(Note7)		{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}			
Receiver					
Signaling Speed per Lane	BR_{AVE}		25.78		Gbps
Data Rate Variation		-100		+100	ppm
Damage threshold	Rxdmg	3.5			dBm
Lane_0/4 Center Wavelength	λ_{C0}	1264.5		1277.5	nm
Lane_1/5 Center Wavelength	λ_{C1}	1284.5		1297.5	nm
Lane_2/6 Center Wavelength	λ_{C2}	1304.5		1317.5	nm
Lane_3/7 Center Wavelength	λ_{C3}	1324.5		1337.5	nm

Optical Characteristics

Average receive power *(Note8)	Rxpow	-13		2.5	dBm
Receive Power (OMA) per Lane	RxOMA			2.5	dBm
Unstressed Receiver Sensitivity (OMA) per Lane *(Note9)	Rxsens			-11.5	dBm
Stressed Receiver Sensitivity (OMA) per Lane *(Note10)	RX_{SRS}			-8.6	dBm
Optical Return Loss	ORL			-26	dB
Conditions of stressed receiver sensitivity test					
Vertical Eye Closure Penalty *(Note11)	VECP	2.6			dB
Stressed J2 Jitter *(Note11)	J2	0.33			UI
Stressed J4 Jitter *(Note11)	J4	0.48			UI
SRS eye mask definition {X1, X2, X3, Y1, Y2, Y3} *(Note11)		{0.39, 0.5, 0.5, 0.39, 0.39, 0.4}			
LOS Assert	LOSA	-25			dBm
LOS De-Assert	LOSD			-15	dBm
LOS Hysteresis		0.5			dB

Note3: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note4: Even if the TDP < 1.0dB, the OMA (min) must exceed this value.

Note5: TDP does not include a penalty for multi-path interference (MPI).

Note6: Transmitter reflectance is defined looking into the transmitter.

Note7: Hit ratio of $5x10^{-5}$

Note8: Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

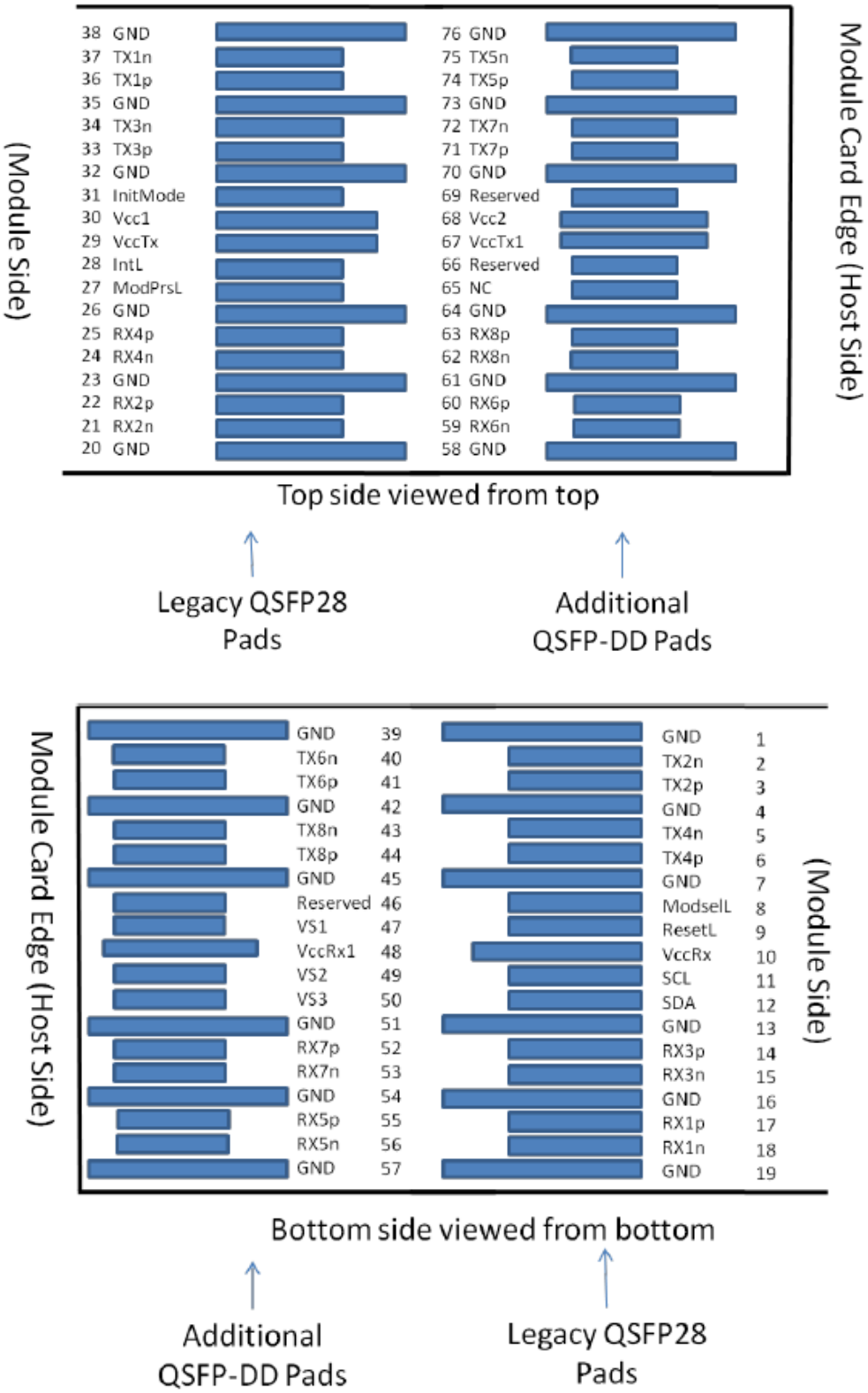
Note9: Sensitivity is specified at $5x10^{-5}$ BER.

Note10: Measured with conformance test signal at TP3 for BER = $5x10^{-5}$.

Note11: Vertical eye closure penalty, stressed eye J2 Jitter, stressed eye J4 Jitter, and SRS eye mask definition are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

networks

QSFP-DD Transceiver Electrical Pad Layout



Pin	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS- I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power Mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pin Arrangement and Definition

39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1
1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.					
2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. VccRx, VccRx1,					

Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

Mechanical Specifications