QSFP-DD800 8x100G LR 10km SMF Optical Transceiver

D-DP8CNL-N00

Product Specification

Preliminary

Features

- QSFP-DD MSA compliant
- CMIS 5.0 Fully compliant
- Parallel 8 Optical Lanes
- 100G Lambda MSA 100G-LR Specification compliant
- Up to 10km transmission on single mode fiber with FEC support at the host
- Operating case temperature: 0 to 70C
- Electrical interface: compliant with 800GAUI-8 (8x106.25Gb/s) interface defined in IEEE 802.3ck
- Rate Date operation at 106.25Gbps (PAM4) per channel
- Maximum power consumption 17W
- MPO-16 connector

Applications

- 800G Ethernet
- Infiniband interconnects
- Datacenter Enterprise networking

Part Number Ordering Information

D-DP8CNL-N00	QSFP-DD800 8x100G LR 10km optical transceiver with MPO-16 connector and with full real-time digital diagnostic monitoring and pull tab

1. General Description

This product is a 800Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) optical module designed for 10km optical communication applications. The module converts 8 channels of 100Gb/s (PAM4) electrical input data to 8 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 800Gb/s. Reversely, on the receiver side, the module converts 8 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 800Gb/s into 8 channels of 100Gb/s (PAM4) electrical output data.

An optical fiber cable with an APC/MPO-16 connector can be plugged into the QSFP-DD 8x100G LR module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through a QSFP-DD MSA-compliant edge type connector.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

2. Functional Description

The module incorporates 8 parallel channels on 1310nm center wavelength, operating at 100G per channel. The transmitter path incorporates a quad channel EML driver integrated in DSP together with 8 parallel EMLs. On the receiver path, a PD array is connected with 2 quad channel TIAs to convert the parallel 800Gb/s optical input into 8 channels of parallel 100Gb/s (PAM4) electrical signals. The electrical interface is compliant with IEEE 802.3ck and QSFP-DD MSA in the transmitting and receiving directions, and the optical interface is compliant to QSFP-DD MSA with MPO-16 connector.

A single +3.3V power supply is required to power up this product. All the power supply pins are internally connected and should be applied concurrently. As per MSA specifications the module offers seven low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, InitMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the

Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Initialize Mode (InitMode) is an input signal. It is pulled up to Vcc in the QSFP-DD module. The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in the QSFP-DD Management Interface Specification. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for LPMode signal description.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a "Low" state.

Interrupt (IntL) is an output pin. "Low" indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface.

The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

3. Transceiver Block Diagram

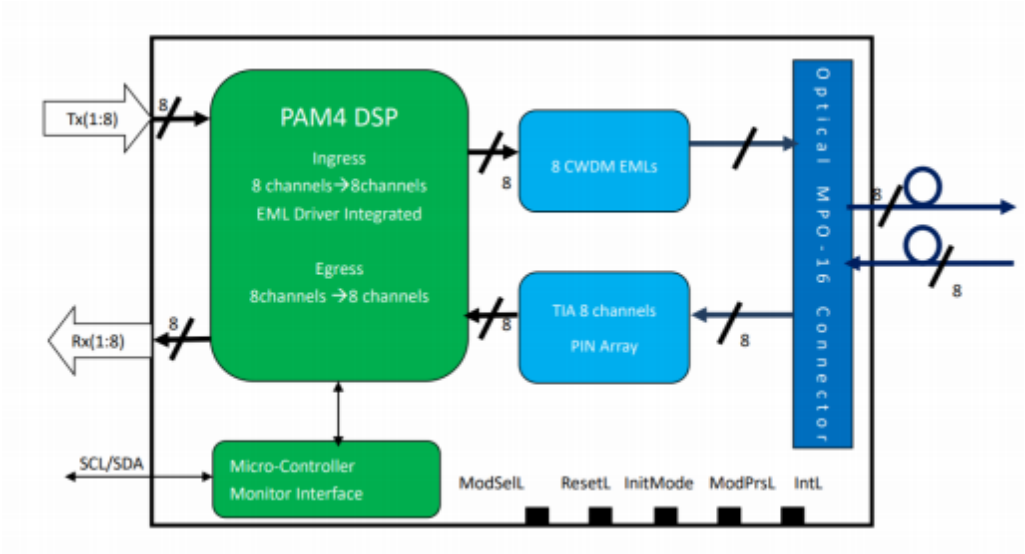

Figure 1. Transceiver Block Diagram

4. Pin Assignment and Description

The electrical pinout of the QSFP-DD module is shown in Figure 2 below.

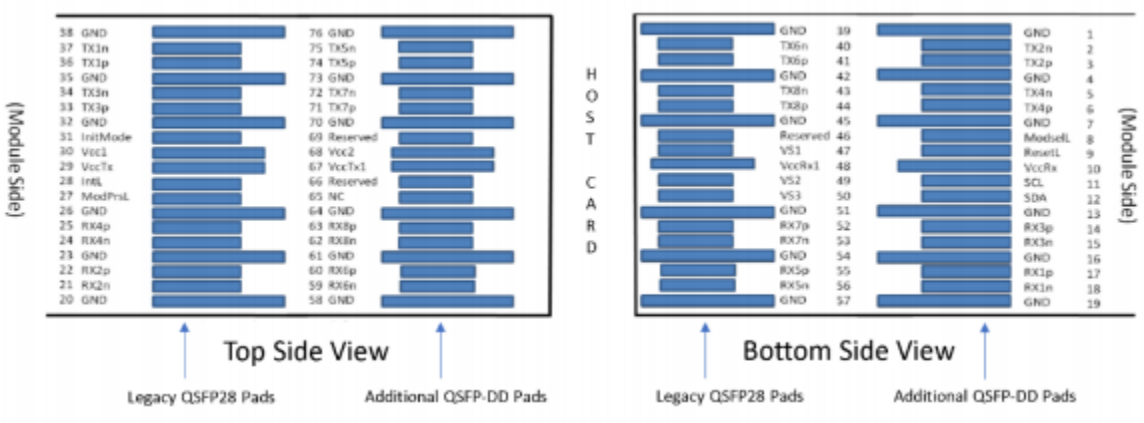

Figure 2. MSA Compliant Connector

Pin Definition

Pin #	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
4		GND	Ground	1B
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B
7		GND	Ground	1B
8	LVTTL-I	ModSelL	Module Select	3B
9	LVTTL-I	ResetL	Module Reset	3B
10		VccRx	+3.3V Power Supply Receiver	2B
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B
13		GND	Ground	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16	GND	Ground	1B	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B
19		GND	Ground	1B
20		GND	Ground	1B
21	CML-O	Rx2n	Receiver Inverted Data Output	3B
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground	1B

24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground	1B
27	LVTTL-O	ModPrsL	Module Present	3B
28	LVTTL-O	IntL	Interrupt	3B
29		VccTx	+3.3V Power supply transmitter	2B
30		Vcc1	+3.3V Power supply	2B
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B
32		GND	Ground	1B
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
35		GND	Ground	1B
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B
39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
42		GND	Ground	1A
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A
45		GND	Ground	1A
46		Reserved	For future use	3A
47		VS1	Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49		VS2	Module Vendor Specific 2	3A
50		VS3	Module Vendor Specific 3	3A
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
64		GND	Ground	1A
65		NC	No Connect	3A

66		Reserved	For future use	3A
67		VccTx1	3.3V Power Supply	2A
68		Vcc2	3.3V Power Supply	2A
69		Reserved	For Future Use	3A
70		GND	Ground	1A
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A
73		GND	Ground	1A
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A

5. Recommended Power Supply Filter

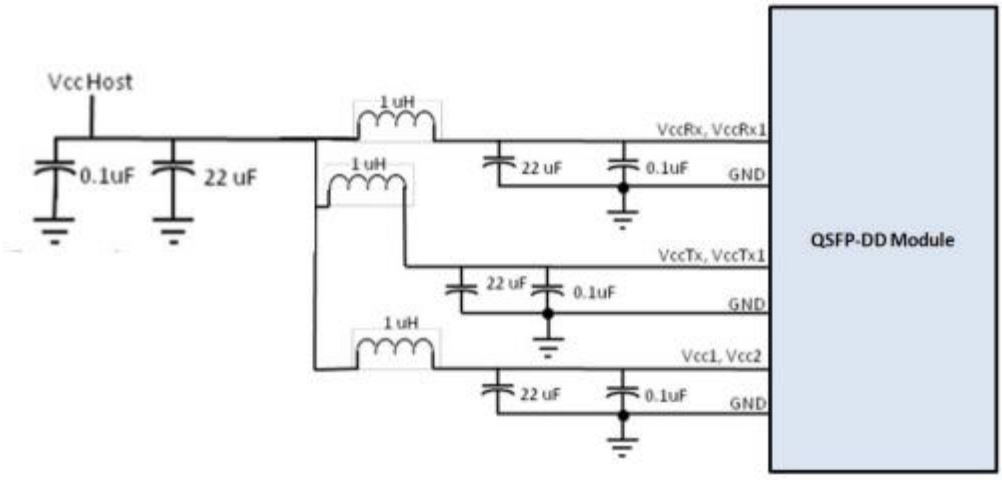

Figure 3. Recommended Power Supply Filter

6. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	degC	
Operating Case Temperature	T_{OP}	0	70	degC	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	
Damage Threshold, each Lane	TH_d	5.8		dBm	

7. Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_{OP}	0		70	degC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance	D	0.2		10000	m	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum transmission distance.

8. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				17	W	
Supply Current	Icc			5.15	A	
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	53.125 ± 100 ppm			GBd	
Differential pk-pk input voltage tolerance	TP1a	750			mV	
AC common-mode RMS voltage tolerance	TP1a	25			mV	
Differential to common-mode return loss, *RLcd*	TP1	Equation(120G-2)			dB	
Effective return loss, ERL	TP1	8.5			dB	
Differential termination mismatch	TP1			10	%	
Module stressed input tolerance	TP1a	See 120G.3.4.3				1
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V	
DC common-mode	TP1	-350		2850	mV	2

voltage						
Receiver (each Lane)						
Signaling Rate, each lane	TP4	53.125 ± 100 ppm			GBd	3
AC common-mode output voltage, RMS	TP4			25	mV	
Differential peak-to-peak output voltage Short mode Long mode	TP4			 600 845	 mV mV	
Eye height, differential		15			mV	
Vertical eye closure				12	dB	
Common-mode to differential return loss	TP4	Equation(120G-1)			dB	
Effective return loss, ERL		8.5			dB	
Differential termination mismatch	TP4			10	%	
Transition time (20% to 80%)	TP4	8.5			ps	
DC common-mode output voltage	TP4	-350		2850	mV	2

Notes:

1. Meets BER specified in 120G.1.1.
2. DC common-mode voltage generated by the host. Specification includes effects of ground offset voltage.
3. The signaling rate range is derived from the PMD receiver input.

9. Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Center Wavelength	λc	1304.5	1310	1317.5	nm	
Transmitter						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				
Side-mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each Lane	P_{AVG}	-1.9		4.8	dBm	1
Outer Optical Modulation	P_{OMA}	Max(1.1,-		5	dBm	2

Amplitude (OMA_{outer}), each Lane		0.3+TDECQ)				
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			3.4	dB	
Transmitter eye closure for PAM4 (TECQ), each Lane	TECQ			3.4	dB	
|TDECQ-TECQ|				2.5	dB	
Over/under-shoot				22	%	
Transmitter power excursion				2.8	dBm	
Extinction Ratio	ER	3.5			dB	
$RIN_{15.6}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	TOL			15.6	dB	
Transmitter Reflectance	R_T			-26	dB	3
Transmitter Transition Time				17	ps	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-15	dBm	
Receiver						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				
Damage Threshold, each Lane	TH_d	5.8			dBm	4
Average Receive Power, each Lane		-8.2		4.8	dBm	5
Receive Power (OMA_{outer}), each Lane				5	dBm	
Receiver Sensitivity (OMA_{outer}), each Lane	SEN			Equation (1)	dBm	6

Stressed Receiver Sensitivity	SRS			-4.1	dBm	7

(OMA_{outer}), each Lane						
Receiver Reflectance	R_R			-26	dB	
LOS Assert	LOSA	-15			dBm	
LOS De-assert	LOSD			-9.4	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Conditions of Stress Receiver Sensitivity Test (Note 8)						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test		3.4			dB	

Notes:

1. Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. The values for OMA_{outer}(min) vary with TDECQ. Figure 4 illustrates this along with the values for OMA_{outer}(max).
3. Transmitter reflectance is defined looking into the transmitter.
4. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
5. Average receive power (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
6. Receiver sensitivity (OMA_{outer}) is informative and is defined for a transmitter with a value of TECQ up to 3.4 dB. Receiver sensitivity should meet Equation (1), which is illustrated in Figure 4.

$$RS = \max(-6.1, TECQ - 7.5)\ dBm \quad (1)$$

Where:

RS is the receiver sensitivity, and

TECQ is the TECQ of the transmitter used to measure the receiver sensitivity.

7. Measured with conformance test signal at TP3 for the BER equal to $2.4x10^{-4}$.
8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

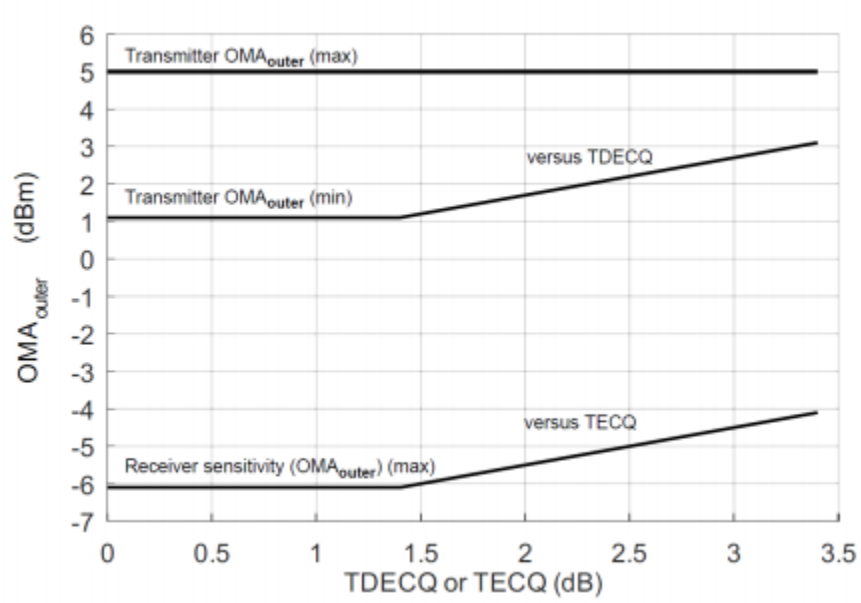

Figure 4. Illustration of Transmitter OMA_{outer} and Receiver Sensitivity Mask for 800G-8x100G LR

10. Digital Diagnostic Functions

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature Monitor Absolute Error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply Voltage Monitor Absolute Error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX Power Monitor Absolute Error	DMI_RX_Ch	-2	2	dB	1
Channel Bias Current Monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX Power Monitor Absolute Error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

11. Mechanical Dimensions

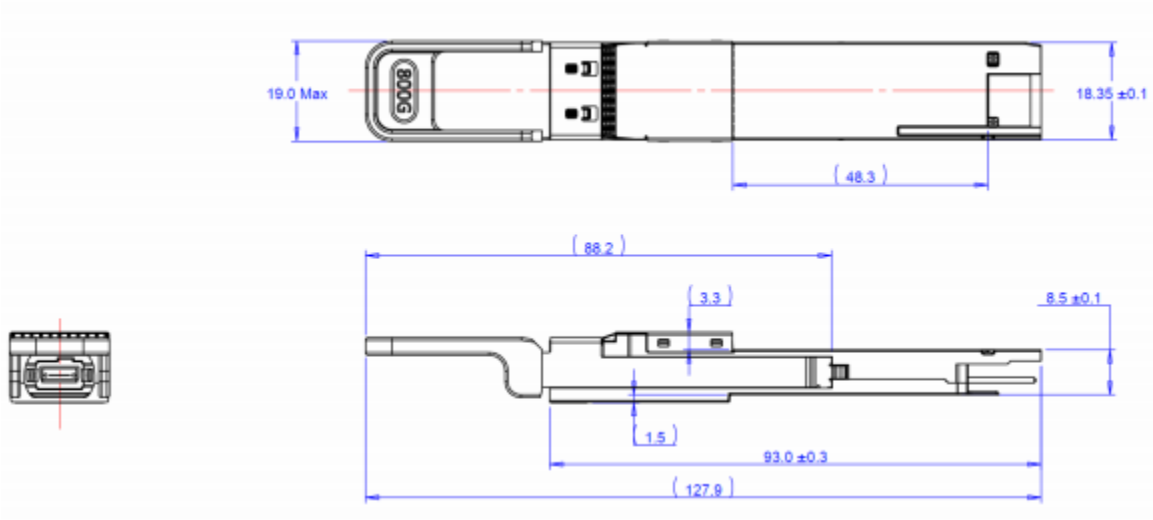

Figure 5. Mechanical Outline

12. ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

13. Laser Safety

This is a Class I Laser Product, or Class 1 Laser Product according to IEC/EN 60825-1:2014.

This product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.