Coherent 400G CFP2 DCO Module

Preliminary Product Specification

Record of Version change：

Date	Version	Flag	Changes	Editor	Auditor	Approver
2020-02-07	V1.0	New	The specification of CFP2 DCO	Jacky		**Alex**
2020-05-12	V1.1	Add	Add OHIO Information	Jacky		**Alex**

Note for column of Flag：

New – First writing of documents.
Add – The document is rewritten for the main purpose of adding new content.
Modify – The document is rewritten for the main purpose of modifying the error.
Upgrade – The whole document has been upgraded, designed to a larger change.

Contents

1. Introduction

This document describes the product specifications for coherent 400G CFP2 DCO modules based on dual polarization quadrature amplitude modulation (DP-16QAM) or probabilistic constellation shaping quadrature amplitude modulation (PCS-16QAM) supporting extended C-band, polarization diversity coherent detection and advanced electronic link equalization. The module can accommodate various client signals such as 100/400 Giga-bit Ethernet(4*100GbE/1*400GbE).The module will enable the following system performance and features:

1. Support Flex-grid(>75GHz) channel spacing DWDM infrastructure
2. Support Flexible client-side interfaces:4*100GbE/1*400GbE
3. Support three line-side FEC types:
    1) 400GZR : 60G Baud OIF 400GZR with CFEC
    2) OpenZR+ : 60G Baud using ZR framer with oFEC
    3) SDFEC: 66G Baud SDFEC with probabilistic constellation shaping
4. Framed PRBS generator/checker on the host and network side interfaces
5. Network and client loopback at the near-endian and far-endian point
6. CFP MSA IEEE802.3 Clause 45 compliant MDIO
7. 104pin CFP2 MSA compliant connector
8. Hot Swappable
9. RoHS compliant
10. Compliant to OIF-CFP2-DCO-01.0, October 17, 2018
11. Compliant to CFP MSA Management Interface Specification, Version 2.6 r06a, March 27, 2017

1.1 Typical Application

The application field of the module is wide from Metro(MR) to short haul(ZR) and Data Center Interconnection (DCI). As shown in Figure 1, it is comprised of high-data lanes, a single 3.3V power supply, an MDIO interface for module control and status report, and dedicated alarm and control pins (not shown on the figure 1).

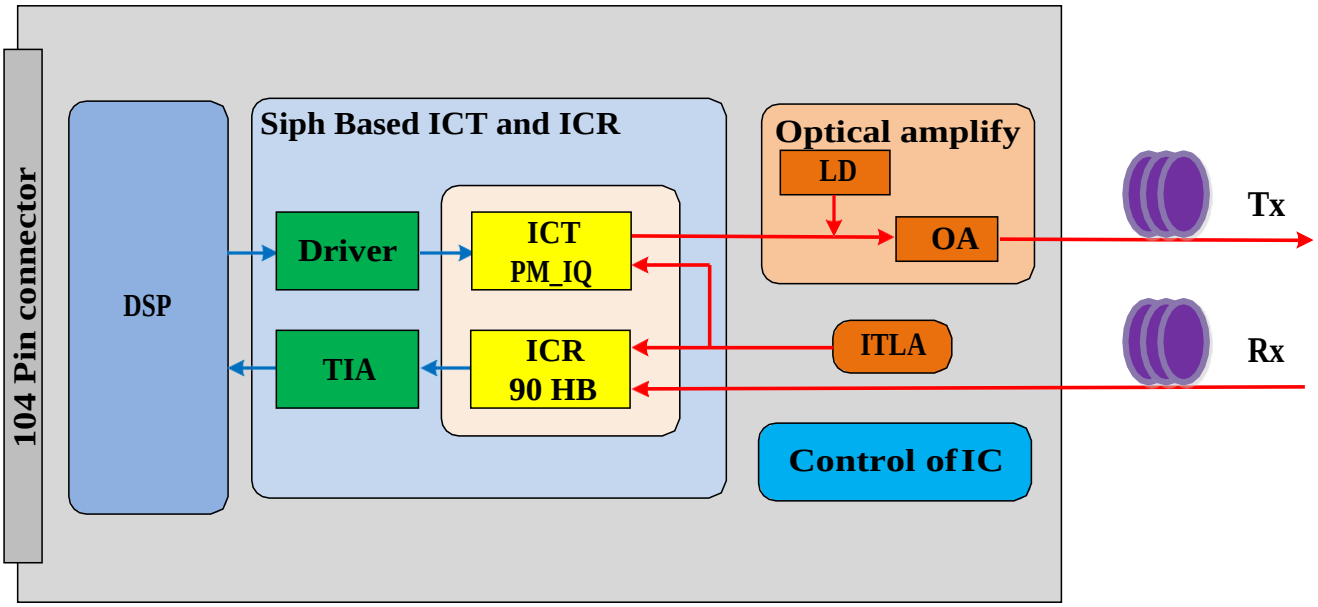

Figure 1: Functional diagram of Module

1.2 Module Description

The Module uses a 104-pin OIF CFP2 Hardware Specification connector (Refer to OIF-CFP2-DCO-01.0.pdf) for all electrical interfaces with the host card, whereas the optical interfaces on the line side are provided through the optical receptacles on the CFP2. The module can be portioned into three functional parts: Tx path, Rx path and Control & Power block.

1.3 Path Description

The host interface is comprised of a total of 8 high-speed SerDes lanes. This allows module to support three interfaces: an independent four 2-Lane mode client interfaces (for 4*100GbE), or a single 8-lane client interface (1*400GbE application).

2. Module Configuration

The module is designed to maximize the number of use-cases in which it can be deployed. Both the host interface as well as the network interface can be configured for different applications.

2.1 Host Interface

The module supports many host signals types: table1 summarizes the supported client and interface modes in the host interface. For CFEC mode, the module support 1*400GUI-8 host interface only. The electrical properties of the host interface are discussed in detail in section 3.

Table 1: Client interface

Client Side type	Client I/F mode	Client lane rate(Gb/s)	Note
1*400G	1*400GAUI-8	8*56Gbps	
4*100G	4*100GAUI-2	8*56Gbps	

The host rate is dependent on the framing type and the supported host rates are shown in the following table.

Table 2: Host Rates

Host Frame	Host Data Bit Rate(Gbps)	Offset(ppm)	Singal
1*400G KP4	1*425	100	Ethernet class
4*100G	4*100	100	Ethernet class

2.2 FEC mode

Line/network side FEC: the module offers two ways of protecting the payload using forward error correction.

1. 400GZR : 60G Baud OIF 400GZR with CFEC
2. OpenZR+ : 60G Baud using ZR framer with oFEC
3. SDFEC: 66G Baud Soft-Decision FEC with 15.4% overhead provides and with probabilistic constellation shaping. A low overhead-concatenated RS FEC outer code is also provided to eliminate Low Density Parity Check (LDPC) BER floor. The total overall line symbol rate resulting from the choice of SDFEC mode, outer FEC selection and others. The information of FEC mode and modulation mode is as following table.

Table 3: Line FEC Type and modulation mode

Id	Application	Modulation	FEC Type	Lane Baud	Grid	OSNR	Note
1	For 400G	DP-16QAM	oFEC(OpenZR+)	60G	75G	23	
2		PCS-16QAM	SDFEC	66G	75G	21	
3		DP-16QAM	CFEC	60G	75G	25	

3. Product Specifications

3.1 Absolute maximum ratings

The absolute maximum ratings given in the table below define the damage thresholds. Hence, the component shall withstand the given limits without any irreversible damage.

Table 4: Absolute Maximum Ratings

Item	Parameter	Condition (1)	Min	Max	Unit
1	Storage Temperature Range		-40	85	℃
2	Storage Humidity	Relative, no-Condensing	-	85	%
3	Case Temperature Range		-10	+70	℃
4	Power supply		-0.3	3.7	V
5	Input power(Optical)	Peak Power		10	dBm

Note: 1.Top=25℃, unless otherwise specified.

3.2 Operating conditions

Table 5: Operating Environment

Item	Parameter	Condition	Symbol	Min	Max	Unit
1	Operating Case Temperature (Top)		T_{case}	0	70	℃
2	Relative humidity Range	Non-condensing	RH	-	85	%
3	Operating Input Optical Power of Signal		P_{sig}	-18	+5	dBm
4	Storage Temperature Range			-40	85	℃

3.3 Electrical Specifications

3.3.1. Power supply

Table 6: Power specifications

Item	Parameter	Condition	Min	Type	Max	Unit
1	3.3V DC Power Supply Voltage		3.2	3.3	3.4	V
2	3.3V DC Power Supply Current				10	A
3	Power Consumption	Low Power			3	W
4	Power Consumption @ CFEC for 400GZR			TBD		W
5	Power Consumption @ oFEC for OpenZR+			TBD		W
	Power Consumption @ SDFEC			TBD		W
6	Inrush current	Power class 4 & 5			250	mA/us
7	Turn-off current	Power class 4 & 5	-250			mA/us
8	Power Supply Noise	DC - 1MHz			2	%
9	Power Supply Noise	1 - 10MHz			3	%

3.3.2. Hardware Control Pins

The control and status reporting functions between a host and a CFP2 module use non-data control and status reporting pins on the 104-pin connector. The control and status reporting pins work together with the MDIO interface to form a complete HOST-CFP2 management interface. The status reporting pins provide status reporting. There are six (6) Hardware Control pins, five (5) Hardware Alarm pins, and six (6) pins dedicated to the MDIO interface. Specification of the CFP2 hardware signaling pins are given in Ref. [1] with the following changes listed in this section. The module supports real-time control functions via hardware pins, listed in table 7 as bellow.

Table 7: Control Pins

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
17	PRG_CNTL1	Programmable Control 1 *MSA Default: TRXIC_RSTn, TX & RX ICs reset,* *"0": reset, "1"or NC: enabled*	I	3.3V LVCMOS	per CFP MSA MIS Ref. [7]		Pull – Up[2]
18	PRG_CNTL2	Programmable Control 2 *MSA Default: Hardware Interlock LSB*	I	3.3V LVCMOS			Pull – Up[2]
19	PRG_CNTL3	Programmable Control 3 *MSA Default: Hardware Interlock MSB*	I	3.3V LVCMOS			Pull – Up[2]
24	TX_DIS	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull – Up[2]
26	MOD_LOPWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull – Up[2]
28	MOD_RSTn	Module Reset, Active Low (invert)	I	3.3V LVCMOS	Enable	Reset	Pull – Down[3]

[2]Pull-Up resistor (4.7 kOhm to 10 kOhm) is located within the CFP2 module

[3]Pull-Down resistor (4.7 kOhm to 10 kOhm) is located within the CFP2 module

3.3.3. Hardware Alarm Pins

The CFP2 Module supports alarm hardware pins as listed in Table 8.

Table 8: Alarm Pins

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
20	PRG_ALRM1	Programmable Alarm 1 *MSA Default: HIPWR_ON*	O	3.3V LVCMOS	Active High per CFP MSA MIS Ref. [7]		
21	PRG_ALRM2	Programmable Alarm 2 *MSA Default: MOD_READY, Ready state has been reached*	O	3.3V LVCMOS			
22	PRG_ALRM3	Programmable Alarm 3 *MSA Default: MOD_FAULT*	O	3.3V LVCMOS			
25	RX_LOS	Receiver Loss of Signal	O	3.3V LVCMOS	Loss of Signal	OK	
27	MOD_ABS	Module Absent	O	3.3V LVCMOS	Absent	Present	Pull Down[2]

3.3.4. Management Interface Pins

The CFP2 Module supports alarm, control and monitor functions via an MDIO bus. Upon module initialization, these functions are available. CFP2 MDIO electrical interface consists of six (6) pins including two (2) pins for MDC and MDIO, three (3) Physical Port Address pins, and the Global Alarm pin.

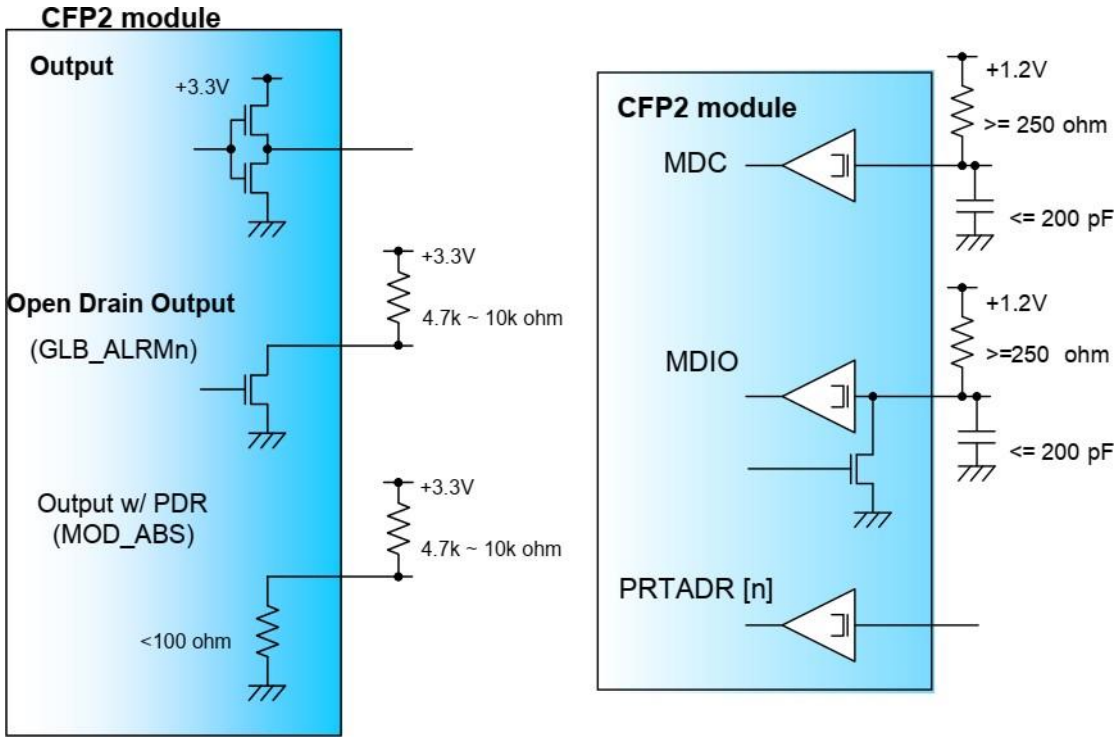

Figure 2: Reference +3.3V LVCMOS Output and MDIO Interface Termination

MDC is the MDIO Clock line driven by the host and MDIO is the bidirectional data line driven by both the host and module depending upon the data directions. The CFP2 MDIO pins are listed in Table 9.

Table 9: Management Interface Pins (MDIO/MDC)

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
29	GLB_ALRMn	Global Alarm	O	3.3V LVCMOS	OK	Alarm	
31	MDC	MDIO Clock	I	1.2V LVCMOS			
32	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS			
33	PRTADR0	MDIO Physical Port address bit 0	I	1.2V LVCMOS	per CFP MSA MIS Ref. [7]		
34	PRTADR1	MDIO Physical Port address bit 1	I	1.2V LVCMOS			
35	PRTADR2	MDIO Physical Port address bit 2	I	1.2V LVCMOS			

3.3.5. Module Management Interface Description

The CFP2 module utilizes MDIO IEEE Std 802.3TM-2012 clause 45 for its management interface. The CFP2 MDIO implementation is defined in a separate document entitled, "OIF-CFP2-DCO-01.0, Revision 1.0, October 17, 2018". When multiple CFP2 modules are connected via a single bus, a particular CFP2 module can be selected by using the Physical Port Address pins.

3.3.6. Overhead I/O Interface (OHIO)

The CFP2 module utilizes 5Gbps SerDes interface for its overhead interface. The relative pins of OHIO are shown in the table 10. The following figure shows OHIO frame that transmits and receives OH data between host and modules.

Table 10: The relative pin of OHIO interface

Pin Number	Name of Pin	Structure (Input/Output)	Logic	Description / Connection
2	OHIO_RDn	O	CML	OHIO output: Differential 100Ω built-in,800-1200mVppd
3	OHIO_RDp	O	CML	OHIO output
5	OHIO_TDn	I	CML	OHIO input: Differential 100Ω built-in,100-1200mVppd
6	OHIO_TDp	I	CML	OHIO input
47	OHIO_REFCLKn	I	CML	OHIO ref clk input, 100MHz, ±100 ppm, 100-1200mVppd
48	OHIO_REFCLKp	I	CML	OHIO ref clk input, Differential 100Ω built-in

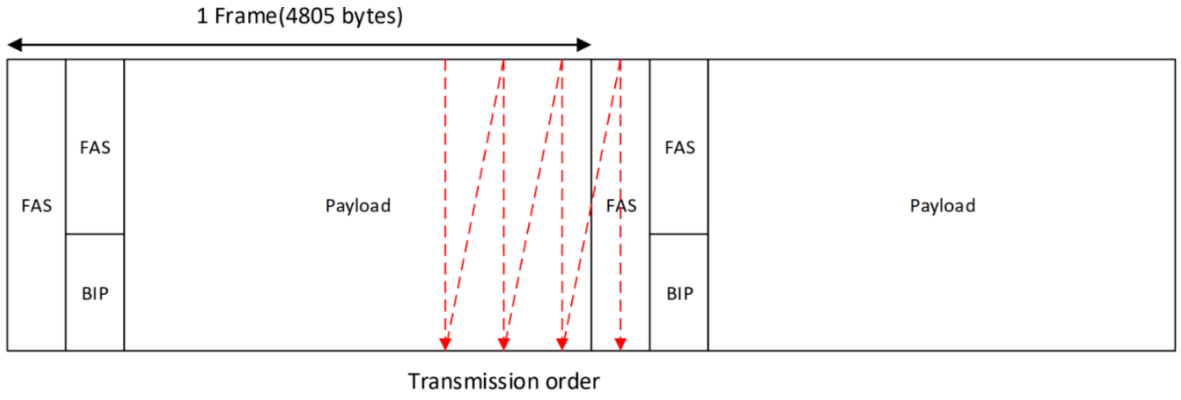

Figure 3: OHIO Frame

Table 11: Each Area of the OHIO Frame

Name	Byte	Discription	Note
FAS	4	Frame Alignment Signal for OHIO Frame	
BIP	1	Result to calculate BIP-8 of the payload in the previous fame	Scrambled field(X^7+X^6+1)
Payload	4800	OHIO data field to be inserted or extracted	

3.4 High-Speed Electrical Specifications

The transmitter and receiver comply with the CEI-56G-VSR-PAM4 electrical specification (OIF-CEI-04.0). The data lines are AC-coupled and terminated in the module per the following figure from the CFP2 MSA.

The Module high speed electrical interface supports the following configurations:

1) 8 tx lanes + 8 rx lanes, each at 56Gbit/s

3.4.1. Loopback

The module support loopback functionality. The host loopback (Loopback ①) and the network loopback (Loopback ②) are shown at bellowing figure. For details on controlling the loopback mode, please refer to Reference [1]. In optional loopback, TXn is looped back to RXn, for example TX0+ to RX0+, on both host and network side.

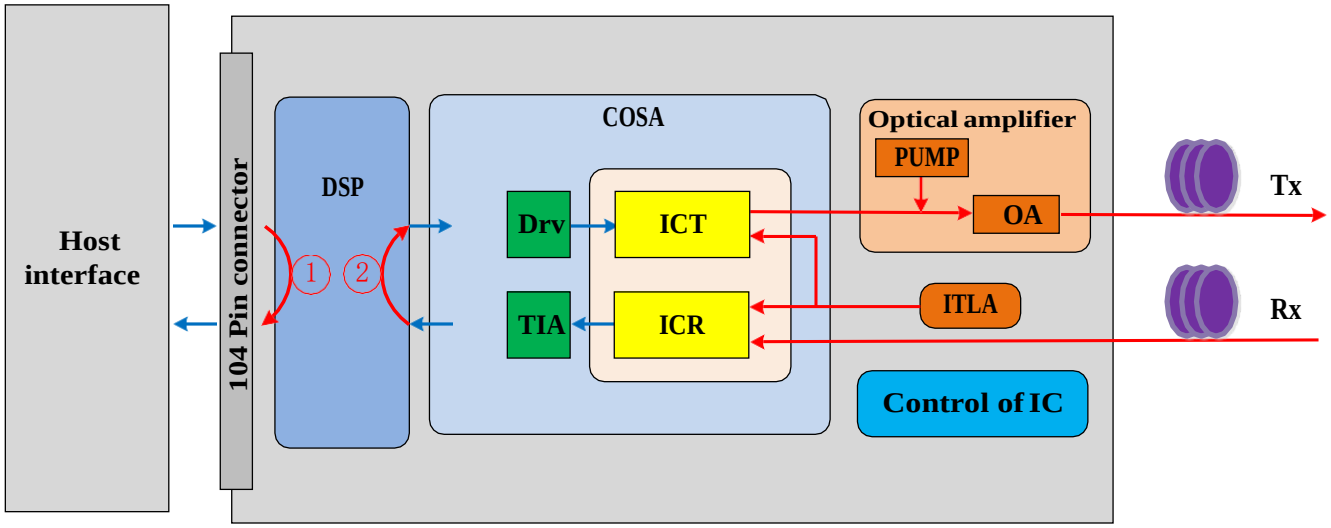

Figure 4: Module Loopback Orientation

3.4.2. Reference Clock

There has local reference clock in module, so the pin 78 and pin 79 which the 1/160 reference clock or the 1/32 reference clock is came from can be in disconnected status.

3.5 Optical Specifications

Unless noted all specifications given in this document are End-of-Life numbers and are valid over case temperature from 0℃ to +70℃.

3.5.1. Optical Transmitter Specifications

There are show all Transmitter specifications in the bellow table.

Table 12: Optical Transmitter Specifications

Id	Parameter	Type	Min	Max	Unit	Condition/comments
1	Transmitter Frequency Range		191.3	196.10	THz	C band 50GHz ITU-T grid. Frequency range over which the specifications hold unless noted otherwise.
2	Channel Spacing	75			GHz	
3	Frequency Stability		-1.8	1.8	GHz	Frequency stability relative to ITU grid.
4	Frequency Offset		-1.8	1.8	GHz	
5	Frequency Fine Tuning Range		-6.0	6.0	GHz	
6	Fine Tuning Resolution	100			MHz	
7	Fine Tuning Time			55	s	
8	Channel Tuning Speed			30	s	Warm start
9	Line Width		100	300	kHz	FWHM
10	SMSR (Side mode suppression Ratio)	45	40		dB	Measured over +/-2.5nm range around the target frequency with 0.06nm RBW without modulation.
11	Transmitter output power range		-10	+2	dBm	Transmitter output is settable in steps of 0.1 dB at any power level within the specified frequency range
12	Output power stability		-0.5	0.5	dB	Output power change over temperature and over time, measured over 10ms second intervals.
13	Output power stability(BOL)		-0.5	0.5	dB	Difference over temperature, time, wavelength and aging.
14	Output power accuracy(EOL)		-1	1	dB	Difference between the set value and actual value over aging.
15	Transmitter turn-up time from warm start		-	100	ms	Module is in Ready state. The maximum transmitter turn-up time is counted from de-assert the Tx_disable Pin to full Tx turn-up.
16	Transmitter laser disable time		-	100	ms	Tx is in full turn-up state. The maximum transmitter turn-off time is counted from assert Tx_disable pin
17	Transmitter turn-up time from cold start		-	90	s	Module is in Low_Power mode. The maximum Tx turn-up time is counted from de-assert the Low_power pin and Tx_disable pin to full Tx turn-up.
18	Transmitter OSNR		38		dB/0.1nm	OSNR at transmitter output (in-band)
19	Transmit signal-to-max ASE		35		dB/0.1nm	Signal to the maximum out-of-band ASE level
20	Transmitter optical return loss		27	-	dB	
21	Transmitter output power with TX disabled			-40	dBm	E.g., max output power when changing laser frequency.
22	Transmitter polarization dependent power			1	dB	Power deference between X and Y polarization

3.5.2. Optical Receiver Specifications

Table 13, 14, 15 contains the general receiver specifications for 400G DP-16QAM applications.

Table 13: Optical Receiver Specifications with DP-16QAM at CFEC for 400GZR

Id	parameter	Type	Min	Max	Unit	Condition/comments
1	Receiver Frequency Range		191.3	196.10	THz	C band 50GHz ITU-T grid.
2	Input power range		-15	+5	dBm	Signal power of the selected channel
3	Receiver Sensitivity	-14			dBm	Minimum input power needed to achieve post FEC BER < 10-15 when OSNR > 35dB and internal FEC enabled
4	OSNR Sensitivity	25			dB/0.1nm	At internal FEC threshold (post FEC BER < 10-15), at optimum Input power as specified above.
5	Los assert		-23		dBm	
6	Los de-assert			-21	dBm	
7	Los hysteresis			2	dB	
8	CD Tolerance			2500	ps/nm	With less than 0.5dB OSNR penalty at FEC threshold.
9	DGD tolerance		90		ps	DGD tolerance Under the following conditions: 0.5dB OSNR penalty at FEC threshold;
10	PDL tolerance		3		dB	PDL tolerance under the following conditions: 1) PDL applied before noise loading; 2) Change in SOP is <=50rad/millisecond; 3) With additional 1.5dB OSNR penalty
11	Tolerance to change in SOP		200	-	rad/ms	Tolerance to change in SOP with <0.5dB OSNR penalty at FEC threshold.
12	Input power transient tolerance		5	-	dB	Optical input power transient tolerance Less than 0.5dB OSNR penalty if the received power is within inout power range and rise/fall times of power change (defined by 20-80%) of 50µs or slower.
13	Dispersion reading accuracy		-3%	3%	ps/nm	The receiver reports the amount of dispersion being compensated.
14	DGD reading accuracy		-4	4	ps	The receiver reports the amount of DGD being compensated.
15	Input power reading accuracy		-1	1	dB	The module reports the actual power as received by the module.
16	Optical Return Loss		27		dB	
17	Receiver turn-up time from cold start		-	90	Seconds	Module is in Low_power state and valid Rx input signal is ready. The time from de-assert Low_power pin to full Rx turn-up, given that valid line side signal is ready.

Table 14: Optical Receiver Specifications with DP-16QAM at oFEC for 400G OpenZR+

Id	parameter	Type	Min	Max	Unit	Condition/comments
1	Receiver Frequency Range		191.3	196.10	THz	C band 50GHz ITU-T grid.
2	Input power range		-15	+5	dBm	Signal power of the selected channel
3	Receiver Sensitivity	-18			dBm	Minimum input power needed to achieve post FEC BER < 10-15 when OSNR > 35dB and internal FEC enabled
4	OSNR Sensitivity	23			dB/0.1nm	At internal FEC threshold (post FEC BER < 10-15), at optimum Input power as specified above.
5	Los assert		-21		dBm	
6	Los de-assert			-19	dBm	
7	Los hysteresis			2	dB	
8	CD Tolerance			42000	ps/nm	With less than 0.5dB OSNR penalty at FEC threshold.
9	DGD tolerance		90		ps	DGD tolerance Under the following conditions: 0.5dB OSNR penalty at FEC threshold;
10	PDL tolerance		3		dB	PDL tolerance under the following conditions: 1) PDL applied before noise loading; 2) Change in SOP is <=50rad/millisecond; 3) With additional 1.5dB OSNR penalty
11	Tolerance to change in SOP		200	-	rad/ms	Tolerance to change in SOP with <0.5dB OSNR penalty at FEC threshold.
12	Input power transient tolerance		5	-	dB	Optical input power transient tolerance Less than 0.5dB OSNR penalty if the received power is within inout power range and rise/fall times of power change (defined by 20-80%) of 50μs or slower.
13	Dispersion reading accuracy		-3%	3%	ps/nm	The receiver reports the amount of dispersion being compensated.
14	DGD reading accuracy		-4	4	ps	The receiver reports the amount of DGD being compensated.
15	Input power reading accuracy		-1	1	dB	The module reports the actual power as received by the module.
16	Optical Return Loss		27		dB	
17	Receiver turn-up time from cold start		-	90	Seconds	Module is in Low_power state and valid Rx input signal is ready. The time from de-assert Low_power pin to full Rx turn-up, given that valid line side signal is ready.

Table 15: Optical Receiver Specifications with PCS-16QAM at SDFEC for 400G

Id	parameter	Type	Min	Max	Unit	Condition/comments
1	Receiver Frequency Range		191.3	196.10	THz	C band 50GHz ITU-T grid.
2	Input power range		-15	+5	dBm	Signal power of the selected channel
3	Receiver Sensitivity	-20			dBm	Minimum input power needed to achieve post FEC BER < 10-15 when OSNR > 35dB and internal FEC enabled
4	OSNR Sensitivity	21			dB/0.1nm	At internal FEC threshold (post FEC BER < 10-15), at optimum Input power as specified above.
5	Los assert		-23		dBm	
6	Los de-assert			-21	dBm	
7	Los hysteresis			2	dB	
8	CD Tolerance			42000	ps/nm	With less than 0.5dB OSNR penalty at FEC threshold.
9	DGD tolerance		90		ps	DGD tolerance Under the following conditions: 0.5dB OSNR penalty at FEC threshold;
10	PDL tolerance		3		dB	PDL tolerance under the following conditions: 1) PDL applied before noise loading; 2) Change in SOP is <=50rad/millisecond; 3) With additional 0.5dB OSNR penalty
11	Tolerance to change in SOP		200	-	rad/ms	Tolerance to change in SOP with <0.5dB OSNR penalty at FEC threshold.
12	Input power transient tolerance		5	-	dB	Optical input power transient tolerance Less than 0.5dB OSNR penalty if the received power is within inout power range and rise/fall times of power change (defined by 20-80%) of 50µs or slower.
13	Dispersion reading accuracy		-3%	3%	ps/nm	The receiver reports the amount of dispersion being compensated.
14	DGD reading accuracy		-4	4	ps	The receiver reports the amount of DGD being compensated.
15	Input power reading accuracy		-1	1	dB	The module reports the actual power as received by the module.
16	Optical Return Loss		27		dB	
17	Receiver turn-up time from cold start		-	90	Seconds	Module is in Low_power state and valid Rx input signal is ready. The time from de-assert Low_power pin to full Rx turn-up, given that valid line side signal is ready.

4. Mechanical Specifications

4.1. Mechanical Overview & Dimensions

The CFP2 module is 107.5x41.5x12.4mm in size and is mechanically compliant to the requirements detailed the CFP2 Hardware Specification rev. 1.0. The module is designed to be inserted into a host board with a railing system that includes a heat sink.

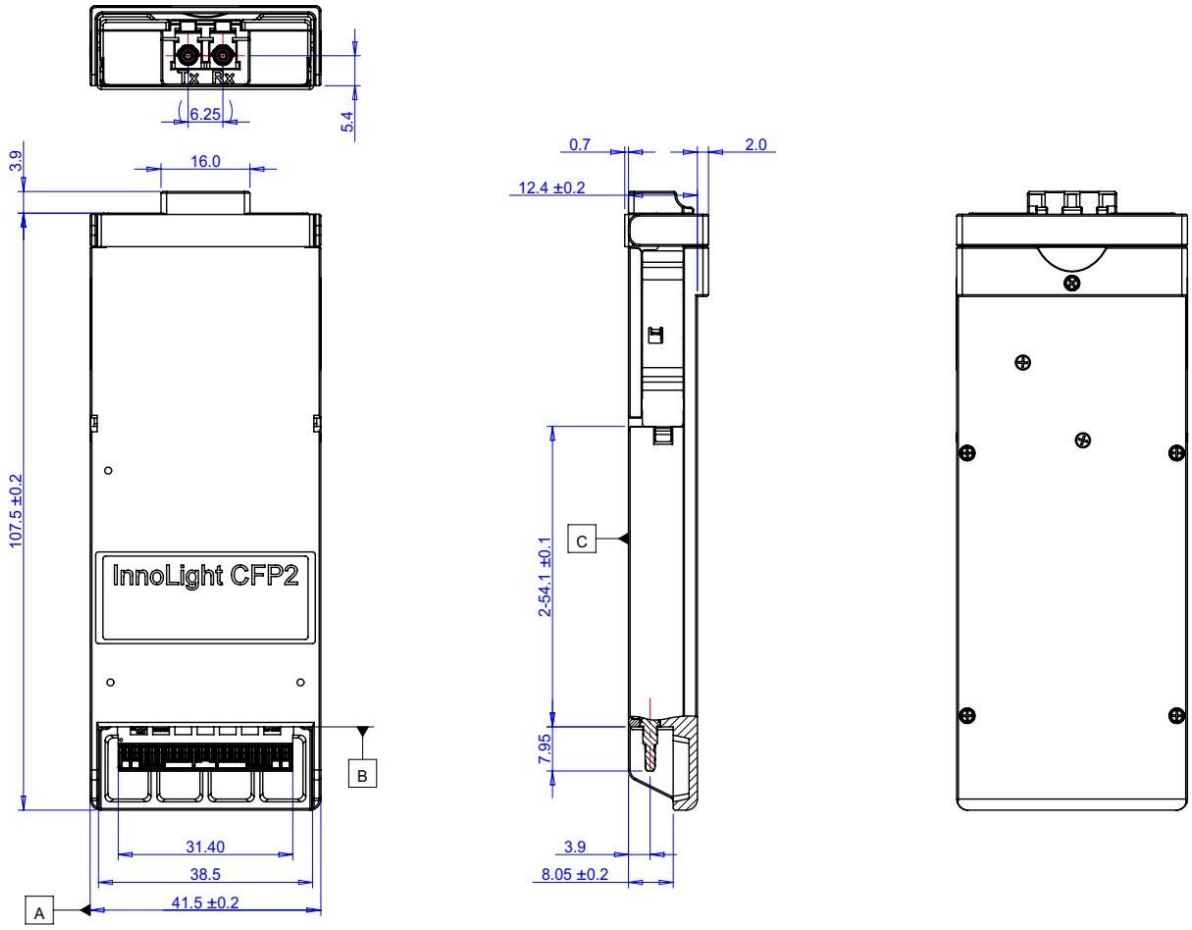

Figure 5: Mechanical Overview for CFP2

4.2. Host Electrical Connector & Pin Assignments

The module plug connector is a sub-component within the CFP2 module. The PCB inserts into the connector with a top and bottom row of pins (primary and secondary side PCB). The host connector has a physical offset of the pin contacts to ensure certain signals make and break contact before others. Ground mates first, the 3.3V and 3.3V ground mate second, the control and status signals mate third, and the MOD_LOPWR, MOD_ABS and high-speed data signals mate last. The module connector is a 104-pin plug connector and the connector pinout defined by the OIF-CFP2-DCO-01.0. All pins are showed as figure 6.

4.2.1. CFP2 Pin-Map

Pin Number	Name of Pin
1	GND
2	OHIO_RDn
3	OHIO_RDp
4	GND
5	OHIO_TDn
6	OHIO_TDp
7	3.3V GND
8	3.3V GND
9	3.3V
10	3.3V
11	3.3V
12	3.3V
13	3.3V GND
14	3.3V GND
15	VND_IO_A
16	VND_IO_B
17	PRG_CNTL1
18	PRG_CNTL2
19	PRG_CNTL3
20	PRG_ALRM1
21	PRG_ALRM2
22	PRG_ALRM3
23	GND
24	TX_DIS
25	RX_LOS
26	MOD_LOPWR
27	MOD_ABS
28	MOD_RSTn
29	GLB_ALRMn
30	GND
31	MDC
32	MDIO
33	PRTADR0
34	PRTADR1
35	PRTADR2
36	VND_IO_C
37	VND_IO_D
38	VND_IO_E
39	3.3V GND
40	3.3V GND
41	3.3V
42	3.3V
43	3.3V
44	3.3V
45	3.3V GND
46	3.3V GND
47	OHIO_REFCLKn
48	OHIO_REFCLKp
49	GND
50	TX_MCLKn
51	TX_MCLKp
52	GND

Pin Number	Name of Pin
104	GND
103	TX4n
102	TX4p
101	GND
100	TX3n
99	TX3p
98	GND
97	TX2n
96	TX2p
95	GND
94	TX5n
93	TX5p
92	GND
91	TX6n
90	TX6p
89	GND
88	TX1n
87	TX1p
86	GND
85	TX0n
84	TX0p
83	GND
82	TX7n
81	TX7p
80	GND
79	(REFCLKn)
78	(REFCLKp)
77	GND
76	RX4n
75	RX4p
74	GND
73	RX3n
72	RX3p
71	GND
70	RX2n
69	RX2p
68	GND
67	RX5n
66	RX5p
65	GND
64	RX6n
63	RX6p
62	GND
61	RX1n
60	RX1p
59	GND
58	RX0n
57	RX0p
56	GND
55	RX7n
54	RX7p
53	GND

Figure 6: CFP2 4*56G or 8*28G bit/s pin-map

The bottom pins of module are descripted as following table.

Table 16: The pin description of Bottom

Pin Number	Name of Pin	Structure (Input/Output)	Logic	Description / Connection
1	GND	GND	Ground	
2	OHIO_RDn	O	CML	OHIO output: Differential 100Ω built-in,800-1200mVppd
3	OHIO_RDp	O	CML	OHIO output
4	GND	GND	Ground	
5	OHIO_TDn	I	CML	OHIO input: Differential 100Ω built-in,100-1200mVppd
6	OHIO_TDp	I	CML	OHIO input
7	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
8	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
9	3.3V	PWR	Power	3.3V Module Supply Voltage
10	3.3V	PWR	Power	3.3V Module Supply Voltage
11	3.3V	PWR	Power	3.3V Module Supply Voltage
12	3.3V	PWR	Power	3.3V Module Supply Voltage
13	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
14	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
15	VND_IO_A	I/O	LVCMOS	Module Vendor I/O. Do Not Connect.
16	VND_IO_B	I/O	LVCMOS	Module Vendor I/O. Do Not Connect.
17	PRG_CNTL1	I	LVCMOS w/PUR	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled or not used
18	PRG_CNTL2	I	LVCMOS w/PUR	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤9W, "01": ≤12W, "10": ≤ 15W, "11" or NC: ≤18W or not used
19	PRG_CNTL3	I	LVCMOS w/PUR	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤9W, "01": ≤12W, "10": ≤15W, "11" or NC:≤18W or not used
20	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1; MSA Default "H" = HIPWR_ON
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2; MSA Default "H" = MOD_READY
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3; MSA Default "H" = MOD_FAULT
23	GND	GND	Ground	
24	TX_DIS	I	LVCMOS w/PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled

25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
26	MOD_LOPWR	I	LVCMOS w/PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
27	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
28	MOD_RSTn	I	LVCMOS w/PUR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
29	GLB_ALRMn	O	LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
30	GND	GND	Ground	
31	MDC	I	1.2V LVCMOS	Management Data Clock (electrical specs as per IEEE Std 802.3- 2012)
32	MDIO	I/O	1.2V LVCMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3-2012)
33	PRTADR0	I	1.2V LVCMOS	MDIO Physical Port Address bit 0
34	PRTADR1	I	1.2V LVCMOS	MDIO Physical Port Address bit 1
35	PRTADR2	I	1.2V LVCMOS	MDIO Physical Port Address bit 2
36	VND_IO_C	I/O	LVCMOS	Module Vendor I/O. Do Not Connect.
37	VND_IO_D	I	LVCMOS	Module Vendor I/O. Do Not Connect.
38	VND_IO_E	I/O	LVCMOS	Module Vendor I/O. Do Not Connect.
39	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply return path.
40	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply return path.
41	3.3V	PWR	Power	3.3V power supply
42	3.3V	PWR	Power	3.3V power supply
43	3.3V	PWR	Power	3.3V power supply
44	3.3V	PWR	Power	3.3V power supply
45	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply return path.
46	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply return path.
47	OHIO_REFCLKn	I	CML	OHIO ref clk input,100MHz, ±100 ppm，100-1200mVppd
48	OHIO_REFCLKp	I	CML	OHIO ref clk input,Differential 100Ω built-in
49	GND	GND	Ground	Module Ground. Logic and power return path
50	TX_MCLKn	O	CML	TX lineside monitor clock
51	TX_MCLKp	O	CML	TX lineside monitor clock
52	GND	GND	Ground	Module Ground. Logic and power return path

Table 17: The pin description of Top

#Pin	Name 8x56G PAM4	Description
104	GND	Ground
103	TX4n	Transmitter lane 4
102	TX4p	
101	GND	Ground
100	TX3n	Transmitter lane 3
99	TX3p	
98	GND	Ground
97	TX2n	Transmitter lane 2
96	TX2p	
95	GND	Ground
94	TX5n	Transmitter lane 5
93	TX5p	
92	GND	Ground
91	TX6n	Transmitter lane 6
90	TX6p	
89	GND	Ground
88	TX1n	Transmitter lane 1
87	TX1p	
86	GND	Ground
85	TX0n	Transmitter lane 0
84	TX0p	
83	GND	Ground
82	TX7n	Transmitter lane 7
81	TX7p	
80	GND	Ground
79	*(REFCLKn)*	N.C
78	*(REFCLKp)*	
77	GND	Ground
76	RX4n	Receiver lane 4
75	RX4p	
74	GND	Ground
73	RX3n	Receiver lane 3
72	RX3p	

71	GND	Ground
70	RX2n	Receiver lane 2
69	RX2p	
68	GND	Ground
67	RX5n	Receiver lane 5
66	RX5p	
65	GND	Ground
64	RX6n	Receiver lane 6
63	RX6p	
62	GND	Ground
61	RX1n	Receiver lane 1
60	RX1p	
59	GND	Ground
58	RX0n	Receiver lane 0
57	RX0p	
56	GND	Ground
55	RX7n	Receiver lane 7
54	RX7p	
53	GND	Ground

4.2.2. High-speed Pin-Map for 400G application

For 400G application, there are three interface modes, which can be supported: 4*100GAUI-2, or 1*400GAUI-8.

Table 18: The pin-map of High-speed pin for 400G application

SerDes Lanes	1*400G	4*100G
	400GAUI-8 (PAM4)	4*100GAUI-2 (PAM4)
	Interface - CH[x,y]	
Tx7[p,n];Rx7[p,n]	CH4.1	CH1.4
Tx6[p,n];Rx6[p,n]		
Tx5[p,n];Rx5[p,n]		CH1.3
Tx4[p,n];Rx4[p,n]		
Tx3[p,n];Rx3[p,n]		CH1.2
Tx2[p,n];Rx2[p,n]		
Tx1[p,n];Rx1[p,n]		CH1.1
Tx0[p,n];Rx0[p,n]		

Note:
1. The CFP2 Host/Client interface naming convention is CH, where, CH=Channel,
2. <x>.<y>:
<x> = channel capacity, where [x=1,2,3,4] is 1=100G, 2=200G, 3=200G or 4=400G.
<y> = channel numeration, where [y=1 …3] is channel numeration.

5. ESD

This transceiver is specified as ESD threshold 250V for according to GR-78 (Human Body Model using C= 100pF, R = 1.5kOhm) on the high speed pins and 500v for all others electrical pins. However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

6. Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

7. Order Information

The part number of coherent module is as descripted as following table.

Table 19: Part number of product

Product	Description	Note
CT-CTS400SMRTA00	Single rate 400Gb/s single channel tunable coherent CFP2 MR(400G DP-16QAM with oFEC), 0 ~ 70°C;	
CT-CTS400SZRTA00	Single rate 400Gb/s single channel tunable coherent CFP2 ZR(400G DP-16QAM with CFEC), 0 ~ 70°C;	

8. Glossary

Table 20: Glossary

Glossary	Info.
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
BS	Beam Splitter
CMRR	Common Mode Rejection Ratio
DSP	Digital Signal Processor
IA	Implementation Agreement
LO	Local Oscillator

MGC	Manual Gain Control
MPD	Monitor Photodiode
MSA	Multi-Source Agreement
OIF	Optical Internetworking Forum
PBS	Polarization Beam Splitter
PCB	Printed Circuit Board
PM-QPSK	Polarization Multiplexed Quadrature Phase Shift Keying
DP-QPSK	Dual Polarization Quadrature Phase Shift Keying
DP-16QAM	Dual Polarization Quadrature Amplitude Modulation
PCS-16QAM	Probabilistic Constellation Shaping Quadrature Amplitude Modulation
OUT4	Optical Transport channel Uint-4
OTUCn	Optical Transport Unit Cn

9. Reference Documents

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[6]. IEEE Std 802.3TM-2012, Annexes 83A, 83B, and 86A.

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[13]. GFEC: ITU-T G.709 standard FEC

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[15]. KR4-FEC: KR4-FEC for 100GbE Client RS(528, 514) -- IEEE802.3 standard Refer to Clause 74, 91

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