100G QSFP-DD DCO Preliminary Product Specification

Document Revision History

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Contents

1. Introduction 6
   1.1 Typical Application 6
   1.2 Module Description 6
   1.3 Path Description 6
2. Module Configuration 7
   2.1 Host Interface 7
   2.2 Media Interface 7
3. Product Specifications 7
   3.1 Absolute Maximum Ratings 7
   3.2 Operating Condition 7
   3.3 Electrical Specifications 8
      3.3.1 Power Supply 8
      3.3.2 Hardware Control and Status Pins 8
      3.3.3 Management Interface 9
   3.4 High Speed Electrical Specifications 10
      3.4.1 Loopback 10
   3.5 Optical Specifications 11
      3.5.1 Optical Transmitter Specifications 11
      3.5.2 Optical Receiver Specifications 12
4. Mechanical Specifications 12
   4.1 Mechanical Overview & Dimensions 12
      4.1.1 Insertion, Extraction and Retention Force 13
   4.2 Host Electrical Connector & Pin Assignments 13
5. Regulatory Specifications 17
   5.1 EMI, EMC and ESD Specification 17
   5.2 Laser Safety 17
6. Order Information 18
7. Contact Information 18

References 19

Abbreviations and Acronyms 20

List of Table

Table 1 Host Interfaces 7
Table 2 Media Interface..... 7
Table 3 Absolute Maximum Ratings 7
Table 4 Operating Condition..... 8
Table 5 Power Supply Specifications 8
Table 6 Optical Transmitter Specifications 11
Table 7 Optical Receiver Specifications 12
Table 8 Insertion, Extraction and Retention Forces..... 13
Table 9 Pad Function Definition 15
Table 10 Host Interface Physical Lane Mapping 17
Table 11 EMI, EMC and ESD Specification 17

List of Figure

Figure 1 Functional Diagram of Module 6
Figure 2 Module Loopback Orientation 11
Figure 3 QSFP-DD Module Mechanical drawing 13
Figure 4 Module pad layout 14

1. Introduction

This document describes the product specifications for 100G QSFP-DD DCO modules based on DP-QPSK, polarization diversity coherent detection and advanced electronic link equalization. Chromatic dispersion compensation can be applied to the receive side of the demodulator. This module is managed utilizing the Two Wire Interface that is specified in the Common Management Interface Specification. The module has following system performance and features:

1) Support Client-side Interfaces with CAUI-4/OTU4
2) Support Line-side interoperable DP-QPSK with GFEC, SCFEC and OFEC
3) Standard QSFP-DD type 2A form factor
4) 76pin QSFP-DD MSA compliant connector
5) Compliant to CMIS 4.0
6) Compliant to OIF Implementation Agreement for Coherent CMIS, Rev 01.1
7) RoHS compliant

1.1 Typical Application

The application field of the module is widely used for short haul and metro haul. As shown in Figure 1, it is comprised of high-data lanes, a single 3.3V power supply, an IIC interface for module control and status report, and dedicated alarm and control pins (not shown on the Figure 1).

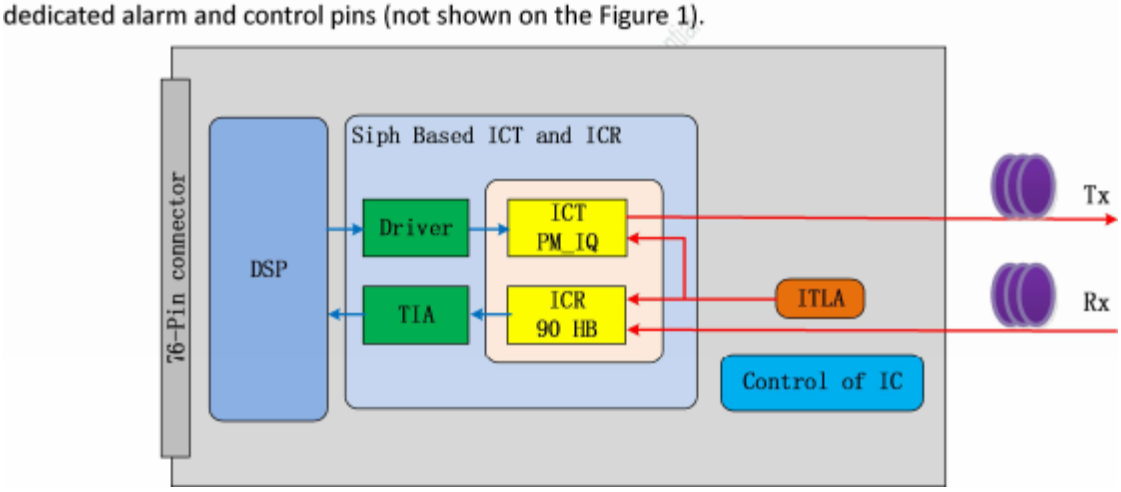

Figure 1 Functional Diagram of Module

1.2 Module Description

The module uses a 76-pin QSFP-DD MSA QSFP-DD Hardware Specificationconnector for all electrical interfaces with the host card, whereas the optical interfaces on the line side are provided through the optical receptacles on the QSFP-DD. The module can be portioned into three functional parts: TX path, RX path and Control & Power block.

1.3 Path Description

The host interface is comprised of a total of 8 high-speed SerDes lanes. This allows module to support interfaces with CAUI-4. The host lane assignment option Lane1-4.

2. Module Configuration

2.1 Host Interface

The module support for wide applications with CAUI-4/OTU4 Host interfaces. The Host interface conform to existing protocol standards and operate over standard physical layer specifications.

Table 1 Host Interfaces

Item	MDI Interface	Application Data Rate	Lane Count	Lane Signaling Rate	Modulation
1	100GE	103.13 Gb/s	4	25.78125 GBaud (+/- 100 ppm)	NRZ
2	OTU4	111.81 Gb/s	4	27.95 GBaud (+/- 20 ppm)	NRZ

2.2 Media Interface

The media interface utilizes DP-QPSK modulation, polarization diversity coherent detection, and advanced electronic link equalization with chromatic dispersion and differential group delay compensation.

Table 2 Media Interface

Item	Payload	Baud Rate	Modulation Format	FEC	Frame
1	100GE/OTU4	27.9525G	DP-QPSK	GFEC	OTU4
2	100GE/OTU4	27.9525G	DP-QPSK	SCFEC	OTU4
3	100GE/OTU4	31.5679G	DP-QPSK	OFEC	OpenROADM
4	100GE	30.0693G	DP-QPSK	OFEC	OpenZR+

3. Product Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings given in the table below define the damage thresholds. Hence, the component shall withstand the given limits without any irreversible damage.

Table 3 Absolute Maximum Ratings

Item	Parameter	Min	Max	Unit	Note
1	Storage Temperature	-40	85	C	
2	Storage Humidity (Relative)	-	85	%	no-Condensing
3	Case Temperature	-5	75	C	
4	Operating Humidity (Relative)	-	85	%	no-Condensing
5	Short term Operating Case Temperature		75	C	
6	Power Supply Absolute Range	-0.3	3.63	V	
7	RX Optical Maximum Input Power		10	dBm	

3.2 Operating Condition

The operating condition given in the table below.

Table 4 Operating Condition

Item	Parameter	Min	Max	Unit	Note
1	Operating Case Temperature	0	70	C	
2	Operating Humidity (Relative)	-	85	%	no-Condensing
3	Power Supply Operating Range	3.135	3.465	V	
4	RX Optical Input Power		2	dBm	

3.3 Electrical Specifications

3.3.1 Power Supply

The 100G QSFP-DD DCO is a Power Class 8 module. In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all QSFP-DD modules shall power up in Low Power Mode if LPMode is asserted. If LPMode is not asserted the module will proceed to High Power Mode without host intervention. Specification values for maximum instantaneous, sustained and steady state currents at each power class are given in Table 5. The power supply requirements are specified in the table below.

Table 5 Power Supply Specifications

Item	Parameter	Min	Typ	Max	Unit	Note
1	3.3V DC Power Supply Voltage	3.135	3.3	3.465	V	
2	Power Dissipation(GFEC)		14.5		W	
3	Power Dissipation(SCFEC)		14.5		W	
4	Power Dissipation(oFEC)		17		W	
5	Low Power Consumption			1.0	W	
6	Module Inrush Current			100	mA/us	
7	Turn-off Current	-100				
8	Power Supply Noise			25	mV	

3.3.2 Hardware Control and Status Pins

In addition to the 2-wire serial interface the module has the following low speed signals for control and status:

- ModSelL
- ResetL
- LPMode
- ModPrsL
- IntL
- ePPS

3.3.2.1 ModSelL

The ModSelL is an input signal that shall be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

3.3.2.2 ResetL

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

3.3.2.3 LPMode

LPMode is an input signal. The LPMode signal shall be pulled up to Vcc in the QSFP-DD module. LPMode is used in the control of the module power mode.

See CMIS Section 6.3.1.3.

3.3.2.4 ModPrsL

ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module. The ModPrsL is asserted "Low" when the module is inserted. The ModPrsL is deasserted "High" when the module is physically absent from the host connector due to the pull-up resistor on the host board.

Low speed signaling other than the SCL and SDA interface is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs. The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

3.3.3 Management Interface

3.3.3.1 General Description

The management communication interface provides a number of elementary management operations that allow the host to read from or write to byte-sized management registers in the management memory map of the module. There are read and write operations both for single bytes and for contiguous byte sequences. Two types of read operations, either with implicit addressing (read from current address) or with explicit addressing, are supported.

The management communication interface distinguishes a master role and a slave role. The host shall be the master and the module shall be the slave.

The master initiates all operations that lead to data transfer. Data can be transferred from the master to the slave (in write operations) and from the slave to the master (in read operations).

3.3.3.2 Physical Layer

The physical layer supporting communication between host and module is the Two Wire serial Interface (TWI).

The TWI consists of a clock signal (SCL) and a data signal (SDA).

SCL and SDA comprise a 2-wire serial interface between the host and module using the TWI protocol. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value shall be 1k ohms to 4.7k ohms depending on capacitive load.

Both signals (SCL and SDA) are bidirectional open-collector pins and require an external pull-up to VCC on the host PCB. Activating the line requires pulling it down (wired AND). The total capacitance on the bus should not exceed 400pF.

The SDA signal is bi-directional. During binary data transfer, the SDA signal shall transition when SCL is low. SDA transitions when SCL is high are used to mark either the beginning (START) or ending (STOP) of a data transfer.

3.3.3.3 Management Interface Timing Specification

.QSFP-DD is positioned to leverage 2-wire timing (Fast Mode devices) to align the use of related cores on host ASICs. The default clock rate is a maximum of 400 kHz with an option to support up to a maximum of 1 MHz. This subsection closely follows the QSFP SFF-8636 specification.

The 2-wire serial interface address of the QSFP-DD module is 1010000X (A0h). In order to allow access to multiple QSFP-DD modules on the same 2-wire serial bus, the QSFP-DD includes a module select pad, ModSelL. This input (which is pulled high, deselected in the module) must be held low by the host to select the module of interest and allow communication over the 2-wire serial interface. The module must not respond to or accept 2-wire serial bus instructions unless it is selected.

3.4 High Speed Electrical Specifications

The transmitter and receiver comply with the CEI-28G-VSR for NRZ coding and CEI-56G-VSR-PAM4 for PAM4 electrical specification (OIF-CEI-04.0). The data lines are AC-coupled and terminated in the module per the following figure from the QSFP-DD MSA. The high-speed signals follow the electrical specifications defined in OIF-CEI-04.0.

The high speed signals consist of 8 transmit and 8 receive differential pairs identified as TX[8:1]p / TX[8:1]n and RX[8:1]p / RX[8:1]n.

3.4.1 Loopback

The module support loopback functionality. The host loopback (Loopback ①) and the network loopback (Loopback ②) are shown at bellowing Figure 2. For details on controlling the loopback mode, please refer to Reference [2]. In optional loopback, TXn is looped back to RXn, for example TX0+ to RX0+, on both host and media side.

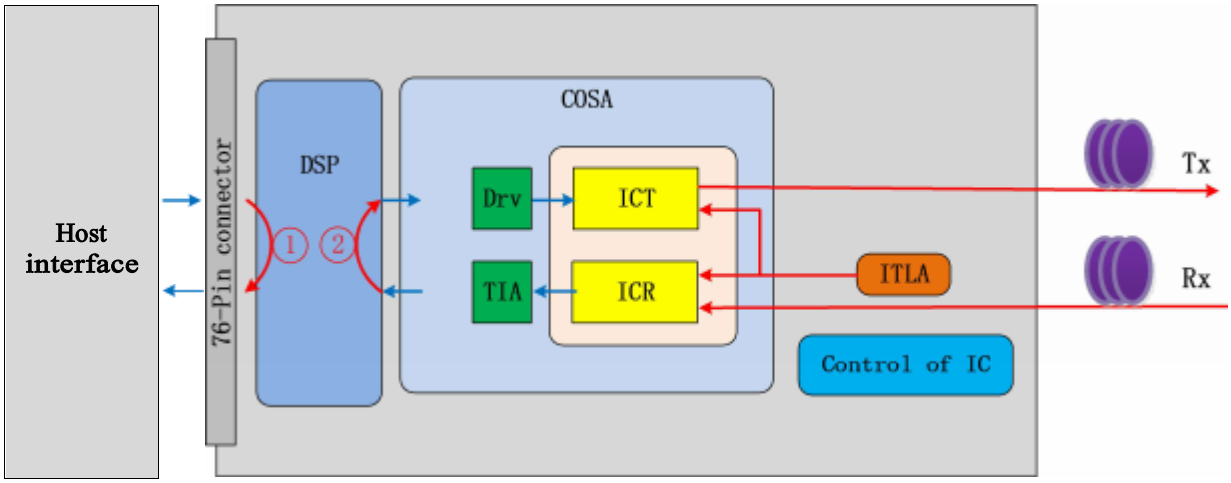

Figure 2 Module Loopback Orientation

3.5 Optical Specifications

All specifications given in this document are End-of-Life numbers and are valid under operating conditions (see Table 4) unless specific noted:

3.5.1 Optical Transmitter Specifications

There are show all Transmitter specifications in the bellow Table 6.

Table 6 Optical Transmitter Specifications

Item	Parameter	Min	Typ	Max	Unit	Condition/comments
1	Transmitter Frequency	193.1	193.7	196.1	THz	
2	Laser Frequency Accuracy	-1.8		1.8	GHz	
3	Laser LineWidth			300	kHz	
4	Transmitter Output Power	-8			dBm	
5	Transmitter Laser Disable Time			180	ms	
6	Output Power Stability	-1		1	dB	Difference over temperature, time, wavelength and aging.
7	Output Power Accuracy	-2		2	dB	Difference between the set value and actual value over aging.
8	Transmitter Turn-up Time from Warm Start	-		180	s	The maximum time from ModuleLowPwr to DataPathActivated state.
9	Transmitter Turn-up Time from Cold Start	-		200	s	
10	Transmitter OSNR (Inband)	38		-	dB/0.1nm	

11	Transmitter Back Reflectance	-		-24	dB	
12	Transmitter Output Power with TX Disabled	-		-20	dBm	

3.5.2 Optical Receiver Specifications

Table 7 shows the general receiver specifications.

Table 7 Optical Receiver Specifications

Item	Parameter	Min	Typ	Max	Unit	Condition/comments
1	Receiver Frequency	191.3	193.7	196.1	THz	
2	Input Power Range	-18		0	dBm	Signal power of the selected channel
3	Receiver Sensitivity (GFEC)		-29		dBm	
4	Receiver Sensitivity (SCFEC)		-30		dBm	
5	Receiver Sensitivity (oFEC)		-32		dBm	
6	OSNR Sensitivity (GFEC)		18.5		dB/0.1nm	
7	OSNR Sensitivity (SCFEC)		15		dB/0.1nm	
8	OSNR Sensitivity (oFEC)		11.5		dB/0.1nm	
9	Los Assert	-30		-28	dBm	
10	Los Hysteresis	1.0		2.5	dB	
11	CD Tolerance(ZR)	2400			ps/nm	Tolerance to Chromatic Dispersion.
12	CD Tolerance(MR)	20000			ps/nm	Tolerance to Chromatic Dispersion.
13	Input Power Transient Tolerance	-2		2	dB	Tolerance to change in input power with < 0.5 dB penalty to OSNR sensitivity.
14	Input Power Reading Accuracy	-2		2	dB	
15	Optical Return Loss	-20			dB	Optical reflectance at Rx connector input.
16	Receiver Turn-up Time from Cold Start	-		100	s	From module reset, with valid optical input signal present.

4. Mechanical Specifications

4.1 Mechanical Overview & Dimensions

The pluggable module fully compliant with the QSFP-DD Type 2a Module Specification, including dimensions

and tolerances for the connector, cage and module system. The module shall be designed to be inserted into a host board with a railing system that includes a heat sink.

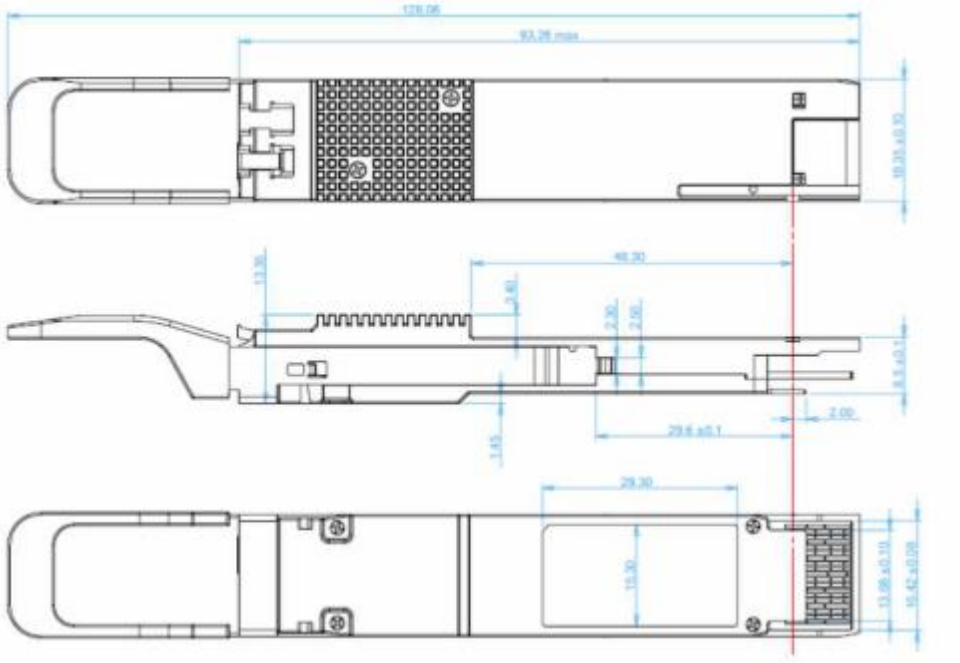

Figure 3 QSFP-DD Module Mechanical drawing

4.1.1 Insertion, Extraction and Retention Force

Table 8 details the mechanical forces to insert, remove, and retain the module in a standard QSFP-DD card cage.

Table 8 Insertion, Extraction and Retention Forces

Item	Parameter	Min	Max	Unit	Note
1	Insertion Force		90	N	
2	Extraction Force		50	N	
3	Retention Force	90		N	

4.2 Host Electrical Connector & Pin Assignments

The electrical interfaces, including pad assignments for data, control, status and power supplies and host PCB layout requirements, of the module is fully compliant with the QSFP-DD MSA QSFP-DD-Hardware Specification, Rev 5.0.

The case of the QSFP-DD module is isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

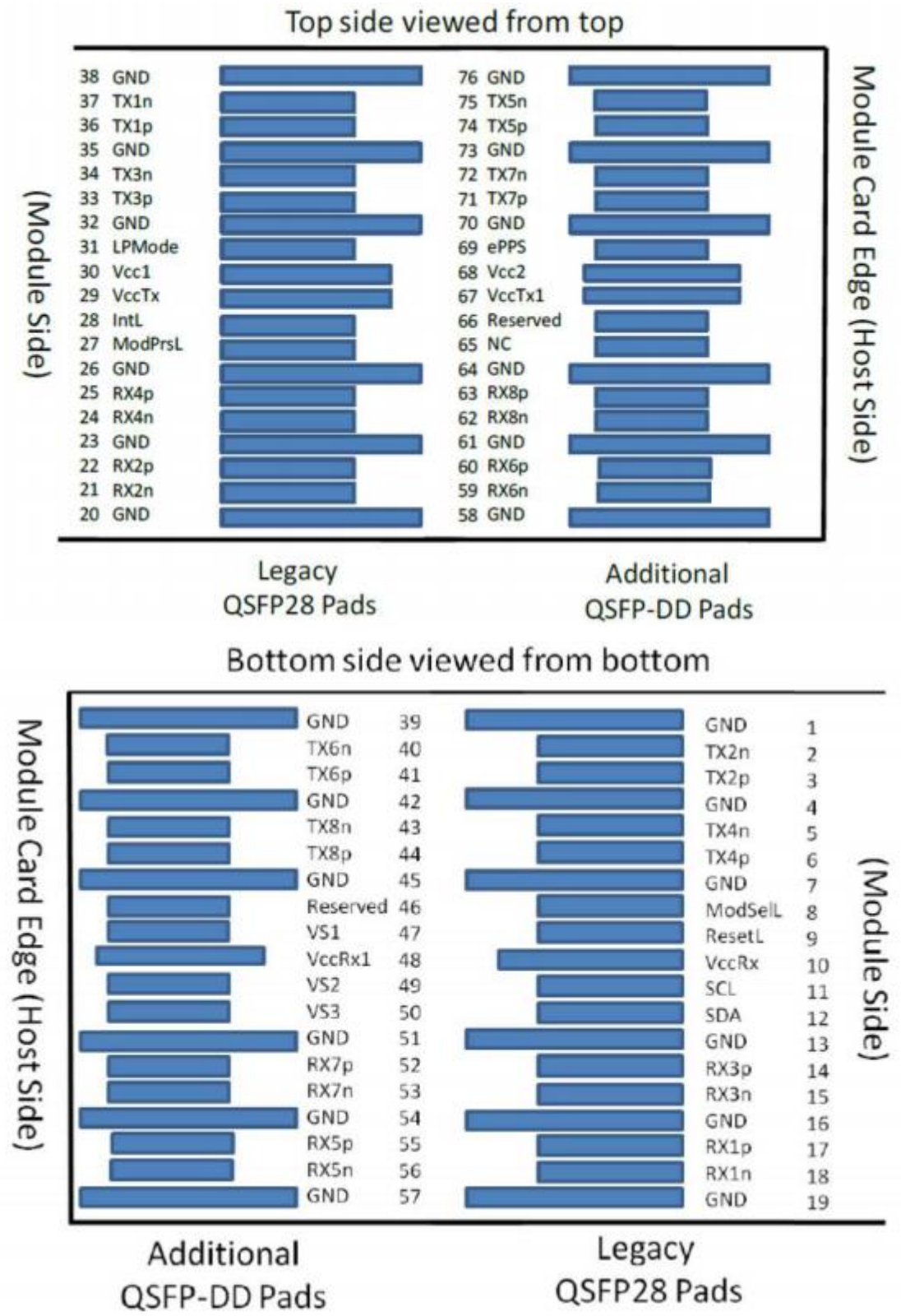

Figure 4 Module pad layout

Table 9 Pad Function Definition

Pin #	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
4		GND	Ground	1B
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B
7		GND	Ground	1B
8	LVTTL-I	ModSelL	Module Select	3B
9	LVTTL-I	ResetL	Module Reset	3B
10		VccRx	+3.3V Power Supply Receiver	2B
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B
13		GND	Ground	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16	GND	Ground	1B	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B
19		GND	Ground	1B
20		GND	Ground	1B
21	CML-O	Rx2n	Receiver Inverted Data Output	3B
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground	1B
24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground	1B
27	LVTTL-O	ModPrsL	Module Present	3B
28	LVTTL-O	IntL	Interrupt	3B
29		VccTx	+3.3V Power supply transmitter	2B
30		Vcc1	+3.3V Power supply	2B
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B
32		GND	Ground	1B
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
35		GND	Ground	1B
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B

39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
42		GND	Ground	1A
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A
45		GND	Ground	1A
46		Reserved	For future use	3A
47		VS1	Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49		VS2	Module Vendor Specific 2	3A
50		VS3	Module Vendor Specific 3	3A
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
64		GND	Ground	1A
65		NC	No Connect	3A
66		Reserved	For future use	3A
67		VccTx1	3.3V Power Supply	2A
68		Vcc2	3.3V Power Supply	2A
69		Reserved	For Future Use	3A
70		GND	Ground	1A
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A
73		GND	Ground	1A
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A

The lane assignments in Table 10 shall be used for the different client signal configurations.

Table 10 Host Interface Physical Lane Mapping

SerDes Lanes	CAUI-4/OTU4	100GAUI-2
Tx8[p,n];Rx8[p,n]	NC	NC
Tx7[p,n];Rx7[p,n]		
Tx6[p,n];Rx6[p,n]		NC
Tx5[p,n];Rx5[p,n]		
Tx4[p,n];Rx4[p,n]	CH1.1	NC
Tx3[p,n];Rx3[p,n]		
Tx2[p,n];Rx2[p,n]		CH1.1
Tx1[p,n];Rx1[p,n]		

Note:

1. The Host/Client interface naming convention is CH, where, CH=Channel,
2. <x>.<y>:

   <x> = channel capacity, where [x=1,2] is 1=100G

   <y> = channel numeration, where [y=1 …3] is channel numeration.

3.NC – No connected

5. Regulatory Specifications

5.1 EMI, EMC and ESD Specification

The module is compliant with the requirements listed in the table below when installed in the host equipment.

Table 11 EMI, EMC and ESD Specification

Item	Parameter	Reference	Value	Unit	Note
1	ESD Immunity	IEC 61000-4-2	8	kV	Contact Discharge
			15	kV	Air Discharge
2	ESD (HBM model)	JEDEC JESD22-A114-B	1	kV	High-Speed Contacts
			2	kV	Other pins
3	EMC Immunity	IEC 61000-4-3			
4	EMI Emission	FCC Class B			

5.2 Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Don't directly look into the transmitter fiber connector at any time while the module is in operation.

6. Order Information

The part number of 100G QSFP-DD DCO is as descripted as following table.

Part Number	Description
CT-QDS100SZRTA00	Single rate 100Gb/s, single channel fixed frequency coherent QSFP-DD ZR, 0~70C
CT-QDS100SMRTA00	Single rate 100Gb/s, single channel fixed frequency coherent QSFP-DD MR, 0~70C

References

[1] QSFP-DD MSA QSFP-DD-Hardware Specification, Rev 5.0, July 9, 2019.

[2] QSFP-DD MSA Common Management Interface Specification, Revision 4.0, May 8, 2019.

[3] OIF Implementation Agreement for Coherent CMIS, Rev 01.1, June 10, 2020.

[4] Open ZR+ MSA Technical Specification, Rev 1.0, Sept 4, 2020.

[5] OIF Implementation Agreement 400ZR, Rev 1.0, March 10, 2020.

[6] SFF-8636 Specification for Management Interface for Cabled Environments, Rev 2.7, Jan 26, 2016

[7] Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps, 25G+ bps I/O and 56G+ bps. OIF-CEI-04.0, Dec 29, 2017

[8] IEEE 802.3TM-2018.

[9] IEEE P802.3ct – Standard for Ethernet Amendment: Physical Layers and Management Parameters for 100 Gb/s and 400 Gb/s Operation over DWDM (dense wavelength division multiplexing) systems. E.g. 100GBASE-ZR.

[10] ITU-T Recommendation G.709 (2012) Interfaces for the Optical Transport Network (OTN).

[11] ITU-T G.874 Management aspects of optical transport network elements.

[12] ITU-T G.Sup58 Optical transport network module framer interfaces.

[13] IEC 61754-20LC Fiber optic interconnecting devices and passive components – Fibre optic connector interfaces - Part 20: Type LC connectors.

[14] IEC 60825-1: Safety of Laser Products - Part 1: Equipment classification, requirements and user's guide.

[15] IEC 60825-2: Safety of Laser Products - Part 2: Safety of optical fiber communication systems (OFCS).

[16] IEC 60695-2-2, Ed. No. 2.0, Fire hazard testing – Part 2: Test Methods – Section 2 Needle-flame test.

[17] Telcordia GR-468-CORE, Issue No. 2, Generic Reliability Assurance Requirements for Optoelectronic Devices Used in Telecommunications Equipment.

[18] EN 55032, Electromagnetic compatibility of multimedia equipment - Emission requirements.

[19] IEC 61340-5-1, Ed. No. 1.0, Electrostatics - Part 5-1: Protection of electronic devices from electrostatic phenomena - General requirements.

[20] Telcordia GR-1312-CORE, Generic requirements for Optical Fiber Amplifiers and Proprietary Dense Wavelength Division Multiplexed Systems

Abbreviations and Acronyms

ADC: Analog to Digital Converter

BER: Bit Error Ratio

BOL: Begin of Life

C2M: Chip-to-Module Interconnect

CAUI: (Chip to) 100 Gb/s Attachment Unit Interface

CD: Chromatic Dispersion

CFEC: Concatenated FEC

DAC: Digital to Analog Converter

DGD: Differential group delay

DM: Delay Measurement

DP-QPSK: Dual Polarization Quadrature Phase Shift Keying

DP-mQAM: Dual Polarization Quadrature Amplitude Modulation (e.g. m=8, 16)

DWDM: Dense Wavelength Division Multiplexing

EOL: End of Life

ESD: Electro-Static Discharge

EMI: Electro-Magnetic Interference

FEC: Forward Error Correction

FLEXE: Flexible Ethernet

FLEXO: Flexible Optical Transport Network

LSB: Least Significant Bit

MSB: Most Significant Bit

NRZ: Non-Return to Zero

NVR: Nonvolatile Register

oFEC: Open FEC

OpenZR+: FlexO/ZR-like frame structure with Open FEC encoding

PMD: Polarization mode dispersion

Q: Quadrature phase component

RIN: Relative Intensity Noise

ROADM: Reconfigurable Optical Add Drop Multiplexer

SMSR: Side Mode Suppression Ratio

SOP: State of polarization

SOPMD: Second Order Polarization Mode Dispersion

TBD: To be defined or to be determined

VR: Volatile Register