100G Coherent CFP DCO Module

Product Specification

Record of Version change：

Date	Version	Flag	Changes	Editor	Auditor	Approver
2019-02-25	V1.0	New	The specification of CFP DCO	**Jacky**		**Alex**

Note for column of Flag：

New – First writing of documents.
Add – The document is rewritten for the main purpose of adding new content.
Modify – The document is rewritten for the main purpose of modifying the error.
Upgrade – The whole document has been upgraded, designed to a larger change.

networks

Contents

1. Introduction

This document describes the product specifications for coherent CFP DCO modules based on DP-QPSK modulation supporting extended C-band, polarization diversity coherent detection and advanced electronic link equalization. The module will enable the following system performance and features:

1. Support 50 GHz channel spacing DWDM infrastructure
2. 100G DP-QPSK Up to 1200km long-haul operation
3. CFP DCO Reach beyond 1200km DP-QPSK over legacy infrastructure under following conditions:
    1) No change to existing line equipment, e.g., no extra amplification required
    2) Use current in-line DCMs
    3) Transmission over mixed fiber types
4. 100G DP-QPSK SDFEC.
5. Support CAUI for 100GE
6. Support OTL4.10 for OTU4 host interface for 100G application
7. Framed PRBS generator/checker on the host and network side interfaces
8. Network and client loopback at the near-endian and far-endian point
9. Embedded OTN framer and MAC/PCS Performance Monitoring
10. Hot Swappable
11. RoHS compliant
12. Compliant to CFP-MSA-HW-Spec-rev1-40
13. Compliant to CFP MSA Management Interface Specification 2.4
14. CFP Class 4

1.1 Typical Application

The module is intended to be used on system integrators host board to support transmission over DWDM links in point to point ZR(80km), Metro and long-haul networks. As shown in Figure 1, it is comprised of high-data lanes, a single 3.3V power supply, an MDIO interface for module control and status report, and dedicated alarm and control pins (not shown on the figure 1).

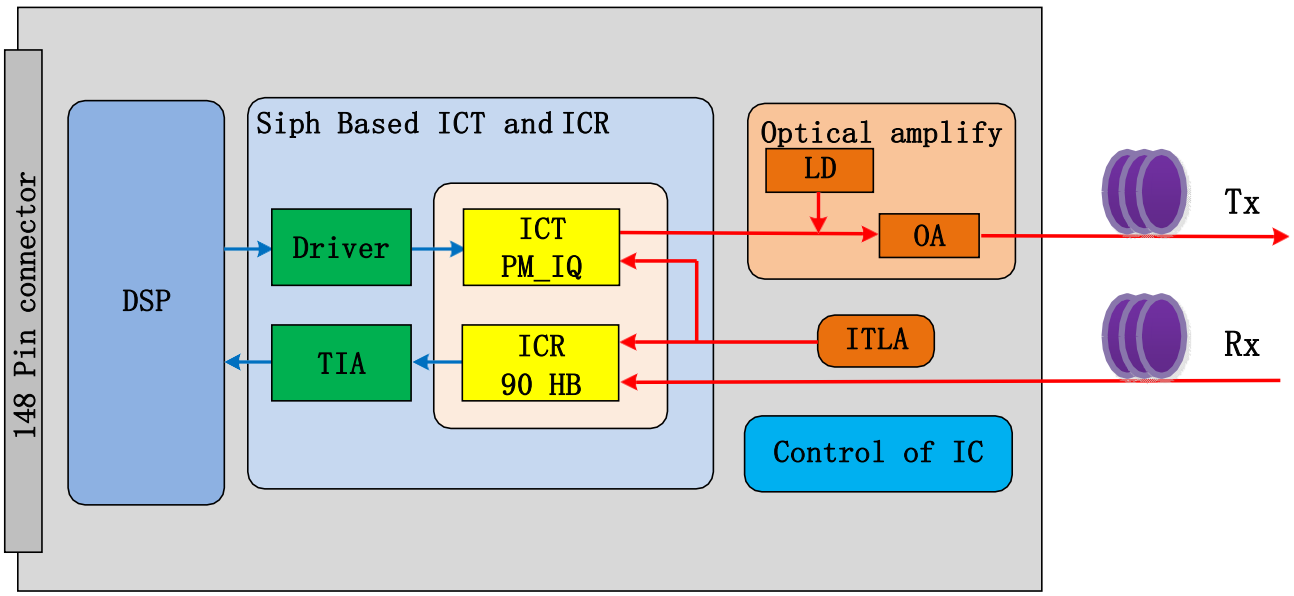

Figure 1: Functional diagram of Module

1.2 Module Description

The Module uses a 148-pin CFP MSA CFP Hardware Specification connector for all electrical interfaces with the host card, whereas the optical interfaces on the line side are provided through the optical receptacles on the CFP. The module can be portioned into three functional parts: Tx path, Rx path and Control & Power block.

1.3 Path Description

The host interface is comprised of a total of 10 high-speed SerDes lanes. This allows module to support a single 10-lane client interface (1xCAUI-10/OTL4.10).

2. Module Configuration

The module is designed to maximize the number of use-cases in which it can be deployed. Both the host interface as well as the network interface can be configured for different applications.

2.1 Host Interface

The module supports many host signal types: table1 summarizes the supported client and interface modes in the host interface. The electrical properties of the host interface are discussed in detail in section 3.

Table 1: Host Rates

Client Side mode	Client I/F mode	Client lane rate(Gb/s)
100GbE	CAUI-10	10x10.3
OTU4	OTL4.10	10x11.18

The host rate is dependent on the framing type and the supported host rates are shown in the following table.

Table 2: Host Rates

Host Frame	Host Data Bit Rate(Gb/s)	Offset(ppm)	Singal
100GE	103.125	100	Ethernet class
OTU4	111.8099736	20	OTU Class

2.2 OTN Framer

The module support ‘terminating modes’ and ‘non-terminating modes (NT)’. The built-in OTN block is responsible for mapping/de-mapping the host signal as well as obtaining frame alignment while monitoring for defects and raising alarms.

2.3 Framing Format

Line/network side SDFEC: Soft-Decision FEC with 20% overhead provides. A low overhead-concatenated RS FEC outer code is also provided to eliminate Low Density Parity Check (LDPC) BER floor. The total overall line symbol rate resulting from the choice of SDFEC mode, outer FEC selection and others.

2.4 FEC Modes

The table below contains a summary of the various FEC modes and B2B OSNR.

Table 3: Line Side FEC modes

Numb.	Modulation	FEC mode	B2B OSNR
1	100G QPSK	20%SDFEC	12.5

2.5 Mapping Modes

2.5.1 Mapping Modes

There are two client modes, which can be supported: 100GE and OTU4. Figure 2 shows the mapping mode supported in one framer/mapper for single-client, 100G applications (100GE/ OTU4). 100GE Ethernet clients are GMP mapped to a standard ODU4 container and after the FEC columns are added, transported towards the line as an OTU4V with either SDFEC encoding. Similarly, OTU4 clients are terminated at the OTU layer and converted to ODU4 which then be transported towards the line as an OTU4V with either SDFEC encoding as figure 3.

2.5.2 Operating modes

The table 4 bellow contains a summary of the various operating modes: four mode for 100G application. There are two operating modes with two 100G client's signal interfaces.

Table 4: Module operating modes for 100G

Numb.	Client I/F Mode	Client Side Mode	Client Side FEC	Client Lane Rate[Gbaud]	Line FEC Mode	Modulation Mode
1	CAUI	100GbE	N/A	10x10.3125	SDFEC	100G QPSK
2	OTL4.10	OTU4	GFEC	10x11.18	SDFEC	100G QPSK

The follow figures bellow contains the various operating modes for 100G applications.

1. Client side: 100GbE(CAUI), OTN OH generations and termination, FEC mode: SDFEC.

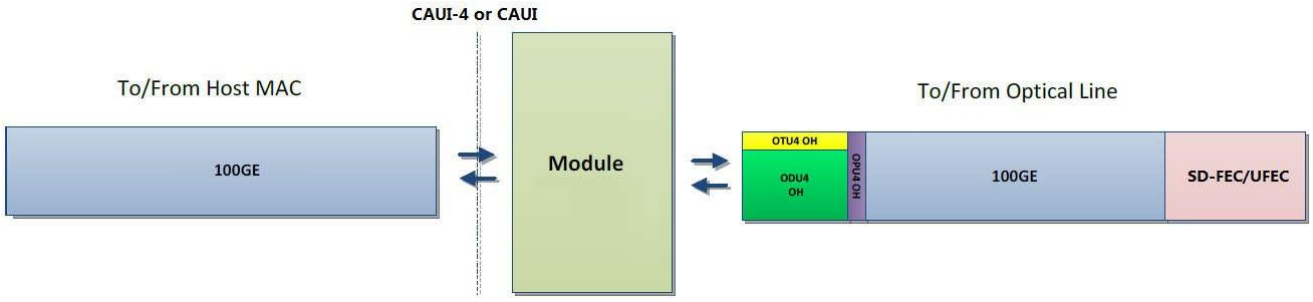

Figure 2: 100GbE operating modes

2. Client side: OTU4(OTL4.10), OTUC1 OH generations and termination, FEC mode: SDFEC.

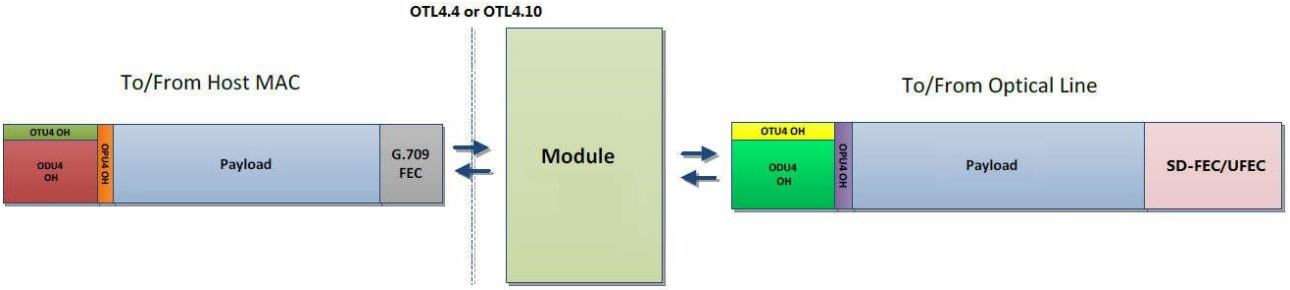

Figure 3: 100G OTU4 operating modes

3. Product Specifications

3.1 Absolute maximum ratings

The absolute maximum ratings given in the table below define the damage thresholds. Hence, the component shall withstand the given limits without any irreversible damage.

Table 5: Absolute Maximum Ratings

Item	Parameter	Condition [1]	Min	Max	Unit
1	Storage Temperature Range		-40	85	℃
2	Storage Humidity	Relative, no-Condensing	-	85	%
3	Case Temperature Range		-10	+75	℃
4	Power supply		-0.3	3.7	V
5	Input power(Optical)	Peak Power		10	dBm

Note: 1.Top=25°C, unless otherwise specified.

3.2 Operating conditions

Table 6: Operating Environment

Item	Parameter	Condition	Symbol	Min	Max	Unit
1	Operating Case Temperature (Top)		T_{case}	-5	70	℃
2	Relative humidity Range	Non-condensing	RH	-	85	%
3	Operating Input Optical Power of Signal		P_{sig}	-18	+5	dBm
4	Storage Temperature Range			-40	85	℃

3.3 Electrical Specifications

3.3.1 Power supply

Table 7: Package configuration

Item	Parameter	Condition	Min	Type	Max	Unit
1	3.3V DC Power Supply Voltage		3.2	3.3	3.4	V
2	3.3V DC Power Supply Current				10	A
3	Power Consumption	Low Power			3	W
4	Power Consumption @100G	Depending on configuration		28	32	W
5	Inrush current	Power class 3 & 4			100	mA/us
6	Turn-off current	Power class 3 & 4	-100			mA/us
7	Power Supply Noise	DC - 1MHz			2	%
8	Power Supply Noise	1 - 10MHz			3	%

3.3.2 Hardware Control Pins

The control and status reporting functions between a host and a CFP module use non-data control and status reporting pins on the 148-pin connector. The control and status reporting pins work together with the MDIO interface to form a complete HOST-CFP management interface. The status reporting pins provide status reporting. There are six (6) Hardware Control pins, five (5) Hardware Alarm pins, and six (6) pins dedicated to the MDIO interface. Specification of the CFP hardware signaling pins are given in Ref. [1] with the following changes listed in this section. The module supports real-time control functions via hardware pins, listed in table 8 as bellow.

Table 8: Control Pins

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
30	PRG_CNTL1	Programmable Control 1 *MSA Default: TRXIC_RSTn, TX & RX ICs reset,* *"0": reset, "1"or NC: enabled*	I	3.3V LVCMOS	per CFP MSA Management Interface Specification [5]		Pull – Up[2]
31	PRG_CNTL2	Programmable Control 2 *MSA Default: Hardware Interlock LSB*	I	3.3V LVCMOS			Pull – Up[2]
32	PRG_CNTL3	Programmable Control 3 *MSA Default: Hardware Interlock MSB*	I	3.3V LVCMOS			Pull – Up[2]
36	TX_DIS	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull – Up[2]
37	MOD_LOPWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull – Up[2]
39	MOD_RSTn	Module Reset (invert)	I	3.3V LVCMOS	Enable	Reset	Pull – Down[3]

3.3.3 Hardware Alarm Pins

The CFP Module supports alarm hardware pins as listed in Table 9.

Table 9: Alarm Pins

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
33	PRG_ALRM1	Programmable Alarm 1 *MSA Default: HIPWR_ON*	O	3.3V LVCMOS	Active High per MDIO document [5]		
34	PRG_ALRM2	Programmable Alarm 2 *MSA Default: MOD_READY, Ready state has been reached*	O	3.3V LVCMOS			
35	PRG_ALRM3	Programmable Alarm 3 *MSA Default: MOD_FAULT*	O	3.3V LVCMOS			
38	MOD_ABS	Module Absent	O	3.3V LVCMOS	Absent	Present	Pull – Down[4]
40	RX_LOS	Receiver Loss of Signal	O	3.3V LVCMOS	Loss of Signal	OK	

3.3.4 Management Interface Pins

The CFP Module supports alarm, control and monitor functions via an MDIO bus. Upon module initialization, these functions are available. CFP MDIO electrical interface consists of eight (8) pins including two (2) pins for MDC and MDIO, (5) Physical Port Address pins, and the Global Alarm pin.

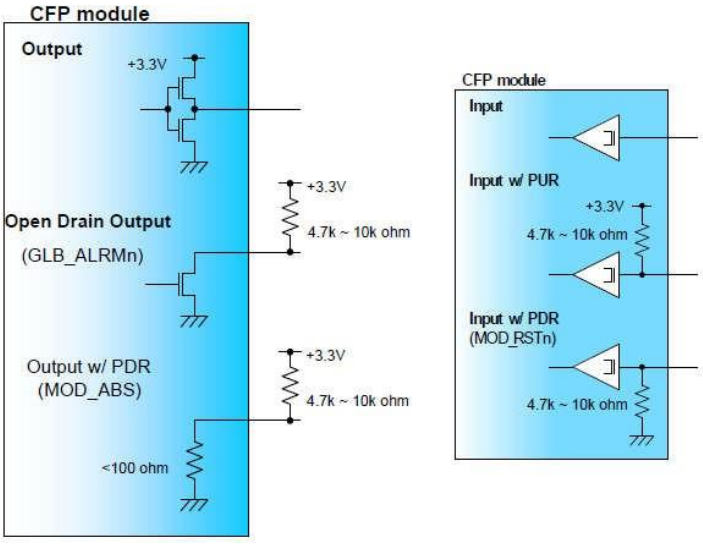

Figure 4: Reference +3.3V LVCMOS Output and MDIO Interface Termination

MDC is the MDIO Clock line driven by the host and MDIO is the bidirectional data line driven by both the host and module depending upon the data directions. The CFP MDIO pins are listed in Table

Table 10: Management Interface Pins(MDIO/MDC)

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
41	GLB_ALRMn	Global Alarm	O	3.3V LVCMOS	OK	Alarm	
47	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS			
48	MDC	MDIO Clock	I	1.2V LVCMOS			
46	PRTADR0	MDIO Physical Port address bit 0	I	1.2V LVCMOS	per MDIO document [5]		
45	PRTADR1	MDIO Physical Port address bit 1	I	1.2V LVCMOS			
44	PRTADR2	MDIO Physical Port address bit 2	I	1.2V LVCMOS			
43	PRTADR3	MDIO Physical Port address bit 3	I	1.2V LVCMOS			
42	PRTADR4	MDIO Physical Port address bit 4	I	1.2V LVCMOS			

3.3.5 Module Management Interface Description

The CFP module utilizes MDIO IEEE Std 802.3TM-2012 clause 45 for its management interface. The CFP MDIO implementation is defined in a separate document entitled, "CFP MSA Management Interface Specification". When multiple CFP modules are connected via a single bus, a particular CFP module can be selected by using the Physical Port Address pins.

3.4 High-Speed Electrical Specifications

The transmitter and receiver comply with the CEI-11G-SR (OIF-CEI-03.1). The data lines are AC-coupled and terminated in the module per the following figure from the CFP MSA. The termination also applies to the reference clock, TX monitor clock, and RX monitor clock.

The Module high speed electrical interface supports the following configurations:

10 tx lanes + 10 rx lanes, each at 10.31 Gbit/s or 11.18Gbit/s.

3.4.1 Loopback (Optional)

The module support loopback functionality. The host loopback(Loopback ①:As be shown on figure5) and the network loopback(Loopback ②: As be shown on figure5) are oriented per Figure 7 shown below. For details on controlling the loopback mode, please refer to Reference [7]. In optional loopback, TXn is looped back to RXn, for example TX0+ to RX0+, on both host and network side.

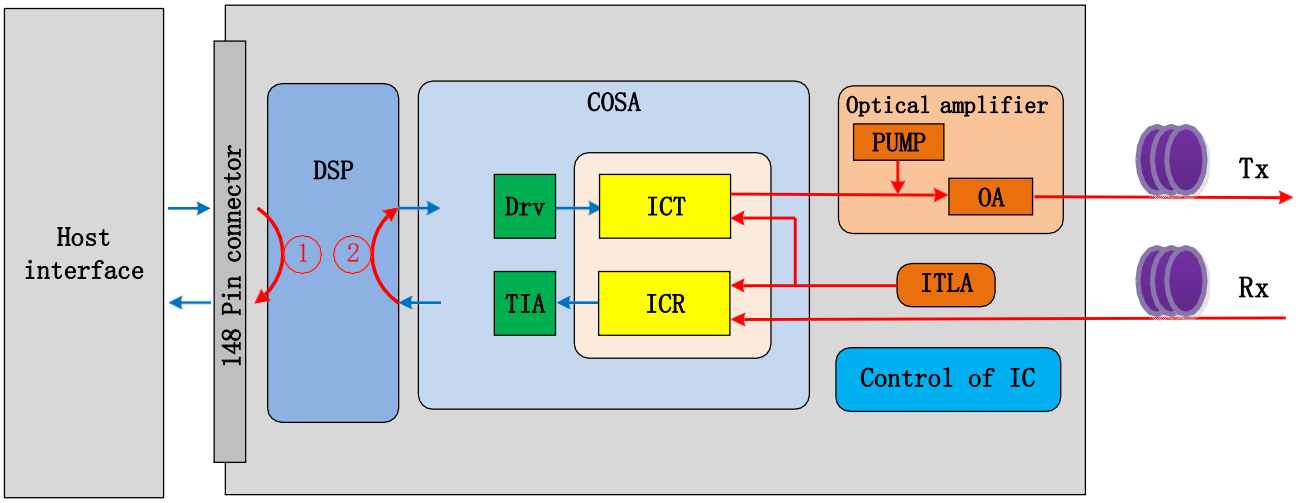

Figure 5: Module Loopback Orientation

3.4.2 Reference Clock (Option)

There has local reference clock in module, so the pin 146 and pin 147 which the 1/16 reference clock or the 1/32 reference clock is came from can be in disconnected status.

3.5 Optical Specifications

Unless noted all specifications given in this document are End-of-Life numbers and are valid over case temperature from -5℃ to +70℃.

3.5.1 Optical Transmitter Specifications

There are show all Transmitter specifications in the bellow table 11.

Table 11: Optical Transmitter Specifications

Id	Parameter	Type	Min	Max	Unit	Condition/comments
1	Transmitter Frequency Range		191.15	196.10	THz	C band 50GHz ITU-T grid. Frequency range over which the specifications hold unless noted otherwise.
2	Channel Spacing	50			GHz	
3	Frequency Stability		-1.8	1.8	GHz	Frequency stability relative to ITU grid.
4	Frequency Fine Tuning Range		-6.0	6.0	GHz	
5	Fine Tuning Resolution	100			MHz	
6	Fine Tuning Time			6	s	
7	Channel Tuning Speed			30	s	
8	Line Width		100	300	kHz	FWHM
9	SMSR (Side mode suppression Ratio)	45	40		dB	Measured over +/-2.5nm range around the target frequency with 0.06nm RBW without modulation.
10	Transmitter output power range		-15	+2	dBm	Transmitter output is settable in steps of 0.1 dB at any power level within the specified frequency range
11	Output power stability		-0.5	0.5	dB	Output power change over temperature and over time, measured over 10ms second intervals.
12	Output power stability(BOL)		-0.5	0.5	dB	Difference over temperature, time, wavelength and aging.
13	Output power accuracy(EOL)		-1	1	dB	Difference between the set value and actual value over aging.
14	Transmitter turn-up time from warm start		-	200	ms	Module is in Ready state. The maximum transmitter turn-up time is counted from de-assert the Tx_disable Pin to full Tx turn-up.
15	Transmitter laser disable time		-	200	ms	Tx is in full turn-up state. The maximum transmitter turn-off time is counted from assert Tx_disable pin
16	Transmitter turn-up time from cold start		-	100	s	Module is in Low_Power mode. The maximum Tx turn-up time is counted from de-assert the Low_power pin and Tx_disable pin to full Tx turn-up.
17	Transmitter OSNR		38		dB/0.1nm	OSNR at transmitter output (in-band)
18	Transmit signal-to-max ASE		35		dB/0.1nm	Signal to the maximum out-of-band ASE level
19	Transmitter optical return loss		27	-	dB	
20	Transmitter output power with TX disabled			-40	dBm	E.g., max output power when changing laser frequency.
21	Transmitter polarization dependent power			1	dB	Power deference between X and Y polarization

3.5.2 Optical Receiver Specifications

Table 12 contains the general receiver specifications for 100G QPSK applications.

Table 12: Optical Receiver Specifications with DP-QPSK and SDFEC for 100G

Id	parameter	Type	Min	Max	Unit	Condition/comments
1	Receiver Frequency Range		191.15	196.10	THz	C band 50GHz ITU-T grid.
2	Input power range		-18	+5	dBm	Signal power of the selected channel
3	Receiver Sensitivity SD-FEC			-24	dBm	Minimum input power needed to achieve post FEC BER < 10-15 when OSNR > 35dB and SDFEC is enabled
4	OSNR sensitivity			12.5	dB/0.1nm	At internal SDFEC threshold (post FEC BER < 10-15), at optimum Input power as specified above.
5	CD Tolerance			40000	ps/nm	with less than 0.3dB OSNR penalty at SD-FEC.
6	DGD tolerance		50		ps	In SD-FEC See note 1 for detail information.
7	PDL tolerance		3		dB	See note 2 for detail information.
8	Tolerance to change in SOP		10	-	rad/ms	Tolerance to change in SOP with OSNR sensitivity specs at SD-FEC threshold.(16KHz)
9	Input power transient tolerance		5	-	dB	See note 3 for detail information.
10	Dispersion reading accuracy		-3%	3%	ps/nm	The receiver reports the amount of dispersion being compensated.
11	DGD reading accuracy		-4	4	ps	The receiver reports the amount of DGD being compensated.
12	Input power reading accuracy		-1	1	dB	The module reports the actual power as received by the module.
13	Optical Return Loss		27		dB	
14	Receiver turn-up time from cold start		-	100	Seconds	Module is in Low_power state and valid Rx input signal is ready. The time from de-assert Low_power pin to full Rx turn-up, given that valid line side signal is ready.

Note:

1. PMD tolerance under the following conditions:
   1) With additional 0.3 dB OSNR from OSNR sensitivity (ID 7 of table). The change in DGD < 45ps per millisecond and change in PSP of < 1 rad/millisecond.
   2) 15ps of PMD corresponds to max 50ps of DGD and max 800 ps2 of SOPMD.
2. PDL tolerance under the following conditions:
   1) No addition PDL from the source
   2) With additional 0.5 dB OSNR from OSNR sensitivity specs (ID 7 of table) Change in PSP is < =1 rad/millisecond

3. Tolerance to variation in received power under the following conditions:
   1) less than 0.5 dB OSNR penalty if the received power is within range defined in “input power range” and rise/fall times of power change (defined by 20-80%) of 50ms or slower.
   2) The OSNR penalty is defined at SD- FEC threshold.

4. Mechanical Specifications

4.1 Mechanical Overview & Dimensions

The CFP module is 155x82x13.60mm in size and is mechanically compliant to the requirements detailed the CFP Hardware Specification rev. 1.0. The module is designed to be inserted into a host board with a railing system that includes a heat sink.

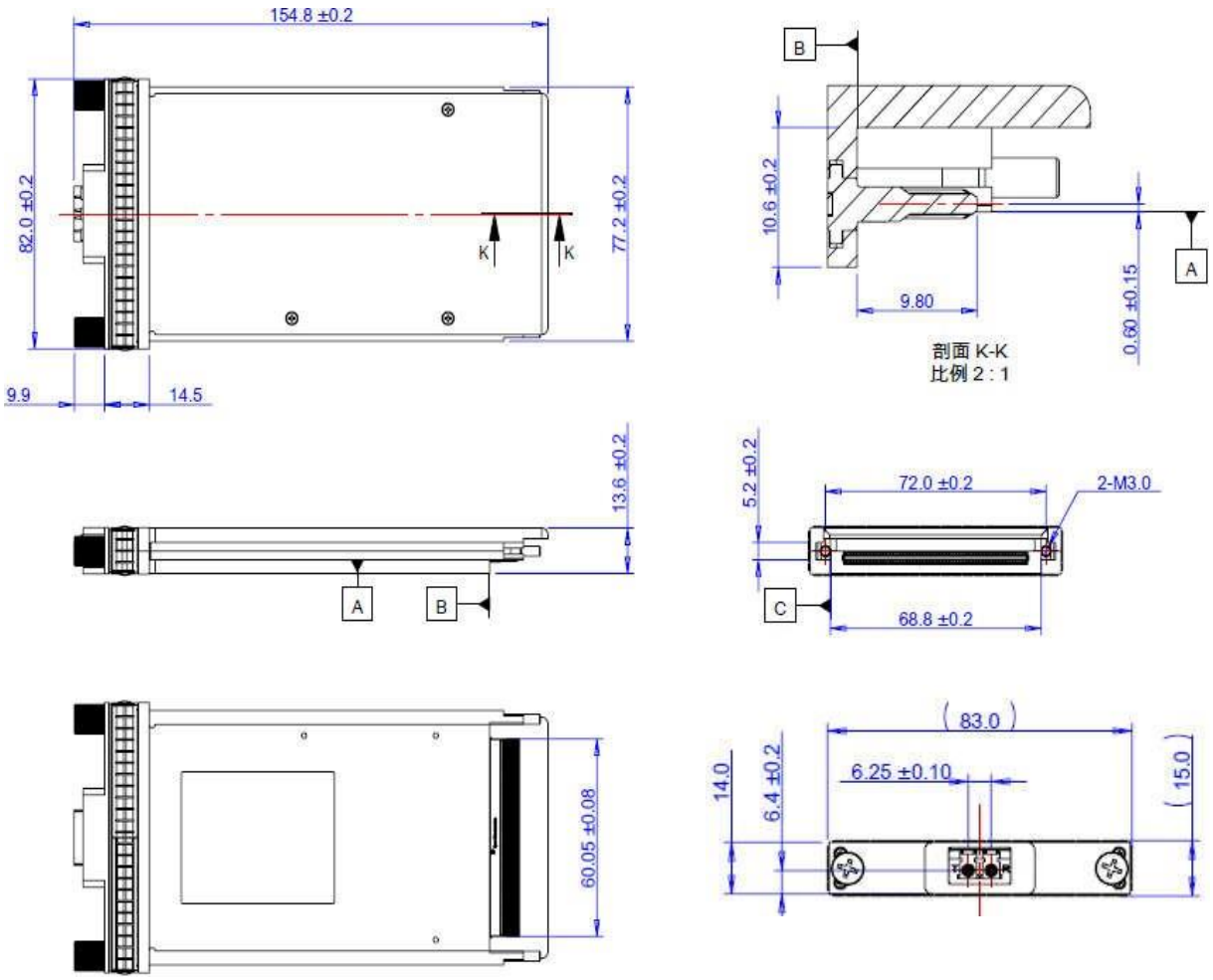

Figure 5: Mechanical Overview for CFP

4.2 Host Electrical Connector & Pin Assignments

The module plug connector is a sub-component within the CFP module. The PCB inserts into the connector with a top and bottom row of pins (primary and secondary side PCB). The host connector has a physical offset of the pin contacts to ensure certain signals make and break contact before others. Ground mates first, the 3.3V and 3.3V ground mate second, the control and status signals mate third, and the MOD_LOPWR, MOD_ABS and high speed data signals mate last. The module connector is a 148-pin plug connector and the connector pinout defined by the CFP MSA.The pin assignments are mechanically compliant to the requirements detailed the CFP Hardware Specification rev. 1.0. All pins are showed as figure 9.

4.2.1 CFP Pin-Map

	Top Row (2nd Half)		Bottom Row (2nd Half)
148	GND	1	3.3V_GND
147	REFCLKn	2	3.3V_GND
146	REFCLKp	3	3.3V_GND
145	GND	4	3.3V_GND
144	*N.C.*	5	3.3V_GND
143	*N.C.*	6	3.3V
142	GND	7	3.3V
141	TX9n	8	3.3V
140	TX9p	9	3.3V
139	GND	10	3.3V
138	TX8n	11	3.3V
137	TX8p	12	3.3V
136	GND	13	3.3V
135	TX7n	14	3.3V
134	TX7p	15	3.3V
133	GND	16	3.3V_GND
132	TX6n	17	3.3V_GND
131	TX6p	18	3.3V_GND
130	GND	19	3.3V_GND
129	TX5n	20	3.3V_GND
128	TX5p	21	VND_IO_A
127	GND	22	VND_IO_B
126	TX4n	23	GND
125	TX4p	24	*(TX_MCLKn)*
124	GND	25	*(TX_MCLKp)*
123	TX3n	26	GND
122	TX3p	27	VND_IO_C
121	GND	28	VND_IO_D
120	TX2n	29	VND_IO_E
119	TX2p	30	PRG_CNTL1
118	GND	31	PRG_CNTL2
117	TX1n	32	PRG_CNTL3
116	TX1p	33	PRG_ALRM1
115	GND	34	PRG_ALRM2
114	TX0n	35	PRG_ALRM3
113	TX0p	36	TX_DIS
112	GND	37	MOD_LOPWR

	Top Row (1st Half)		Bottom Row (1st Half)
111	GND	38	MOD_ABS
110	*N.C.*	39	MOD_RSTn
109	*N.C.*	40	RX_LOS
108	GND	41	GLB_ALRMn
107	RX9n	42	PRTADR4
106	RX9p	43	PRTADR3
105	GND	44	PRTADR2
104	RX8n	45	PRTADR1
103	RX8p	46	PRTADR0
102	GND	47	MDIO
101	RX7n	48	MDC
100	RX7p	49	GND
99	GND	50	VND_IO_F
98	RX6n	51	VND_IO_G
97	RX6p	52	GND
96	GND	53	VND_IO_H
95	RX5n	54	VND_IO_J
94	RX5p	55	3.3V_GND
93	GND	56	3.3V_GND
92	RX4n	57	3.3V_GND
91	RX4p	58	3.3V_GND
90	GND	59	3.3V_GND
89	RX3n	60	3.3V
88	RX3p	61	3.3V
87	GND	62	3.3V
86	RX2n	63	3.3V
85	RX2p	64	3.3V
84	GND	65	3.3V
83	RX1n	66	3.3V
82	RX1p	67	3.3V
81	GND	68	3.3V
80	RX0n	69	3.3V
79	RX0p	70	3.3V_GND
78	GND	71	3.3V_GND
77	*(RX_MCLKn)*	72	3.3V_GND
76	*(RX_MCLKp)*	73	3.3V_GND
75	GND	74	3.3V_GND

Figure 6: CFP 10x10G bit/s pin-map

5. ESD

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kv for all others electrical input pins tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

6. Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

7. Order Information

The part number of CFP DCO module is as descripted as followed table 17.

Table 13: Rules of part number

CT	-	XX	X	XXX	X	XX	X	X	XX
Note1		**Form Factor:** CP: CFP	**Number of Channels:** S: 1 Ch D: 2 Ch	**Data Rate (Single Channel):** 100: 100 Gbit/s 200: 200 Gbit/s	**Rate Select:** S: Single Rate D: Dual Rate T: Triple Rate M: Multi-Rate (supports four rates and above)	**Transmission Distance:** ER: 10~40km ZR: ZR(~100km) MR: MR(~1000km) LH: LR(~2000km) UH: ULH(>2000km)	**Wavelength:** F:Fixed Wavelength; T:C-band Tunable Wavelength;	**Temperature Range:** N: -5 to 60℃ A: -5 to 70℃ E: -10 to 70℃	**Customer Code:** 00: Standard BK: Blank

Note: 1. **CT - Coherent Transceiver**

For examples:

1) CT-CPS100SMRTA00: Single rate 100Gb/s single channel tunable coherent CFP MR, -5～70℃;
2) CT-CPS100SZRTA00: Single rate 100Gb/s single channel tunable coherent CFP ZR, -5～70℃;
3) CT-CPS200SMRTA00: Single rate 200Gb/s single channel tunable coherent CFP MR, -5～70℃;
4) CT-CPS200DMRTA00: Dual rate 200Gb/s single channel tunable coherent CFP MR, -5～70℃;

8. Glossary

Table 14: Glossary

Glossary	Info.
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
BS	Beam Splitter
CMRR	Common Mode Rejection Ratio
DSP	Digital Signal Processor
GBaud	109 Symbols per second
IA	Implementation Agreement
LO	Local Oscillator
MGC	Manual Gain Control
MPD	Monitor Photodiode
MSA	Multi-Source Agreement
OIF	Optical Internetworking Forum
PBS	Polarization Beam Splitter
PCB	Printed Circuit Board
PM-QPSK	Polarization Multiplexed Quadrature Phase Shift Keying

9. Reference Documents

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