

## 400Gb/s OSFP Parallel Active Optical Cable (AOC)

**D-OS8FNMxxx-H00**

### Product Specification

#### Features

- OSFP MSA compliant
- 8 parallel full-duplex channels
- Compliant to IEEE802.3bs
- Up to 100m OM4 MMF transmission
- Operating case temperature: 20 to 60°C
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Data Rate 53.125Gbps (PAM4) per channel.
- Maximum power consumption 10W
- RoHS compliant



#### Applications

- 400G Ethernet
- Infiniband EDR

#### Part Number Ordering Information

D-OS8FNMxxx-H00	OSFP active optical cable with full real-time digital diagnostic monitoring
-----------------	---

where "xxx" denotes cable length in meters. Examples of cable length offered are as follows:

xxx = 001 for 1m

xxx = 050 for 50m

xxx = 005 for 5m

xxx = 075 for 75m



xxx = 010 for 10m

xxx = 100 for 100m

## 1. General Description

This product is a high data rate parallel active optical cable (AOC), to overcome the bandwidth limitation of traditional copper cable. The AOC offers 8 independent data transmission channels and 8 data receiving channels via a multimode fiber cable, each capable of 50Gb/s operation. consequently, an aggregate data rate of 400Gb/s over 100 meters transmission can be achieved by this product, to support the ultra-fast computing data exchange.

The product is designed with form factor, optical/electrical connection according to the OSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

## 2. Functional Description

This product converts the parallel electrical input signals into parallel optical signals (light), by a driven Vertical Cavity Surface Emitting Laser (VCSEL) array. The light propagates through multimode fibers inside the fiber cable individually, and is captured by the photo diode array. The optical signals are converted into parallel electrical signals and outputted. Consequently, each terminal of the cable has 16 ports, 8 for data transmission and 8 for data receiving, to provide totally 400Gb/s data exchange. Figure 2 shows the functional block diagram of the parallel AOC.

A single +3.3V power supply is required to power up this product. As per MSA specifications the module offers 4 low speed hardware control pins: SCL, SDA, INT/RSTn and LPWn/PRSn

SCL and SDA are a 2-wire serial interface between the host and module using the I2C protocol. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value can be 2.2k ohms to 4.7k ohms.

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. Reset is an active-low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-low signal on the host. The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 1 shows these 3 zones.

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host. The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 1 shows these 3 zones.

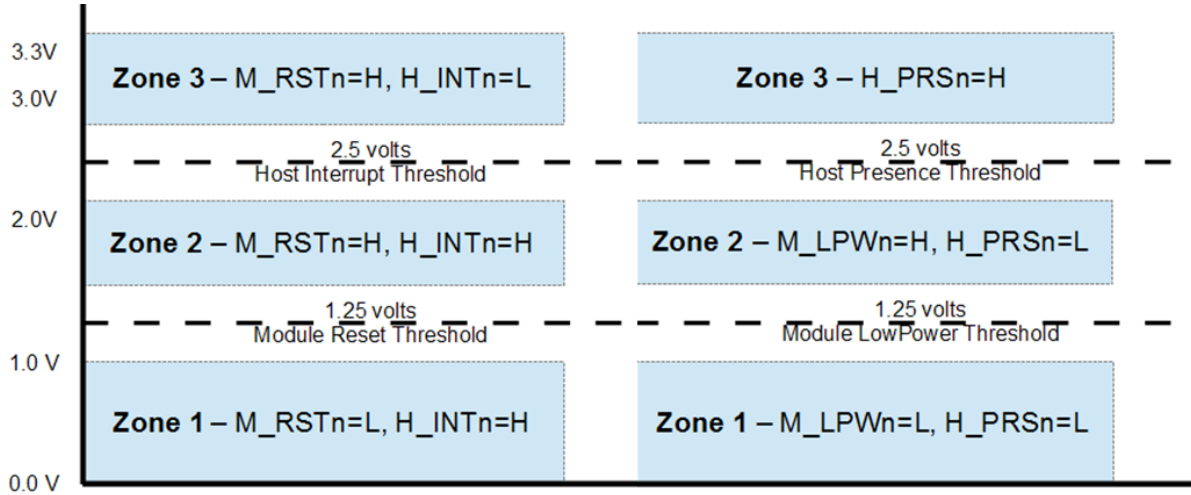


Figure 1. Voltage Zones

### 3. AOC Block Diagram

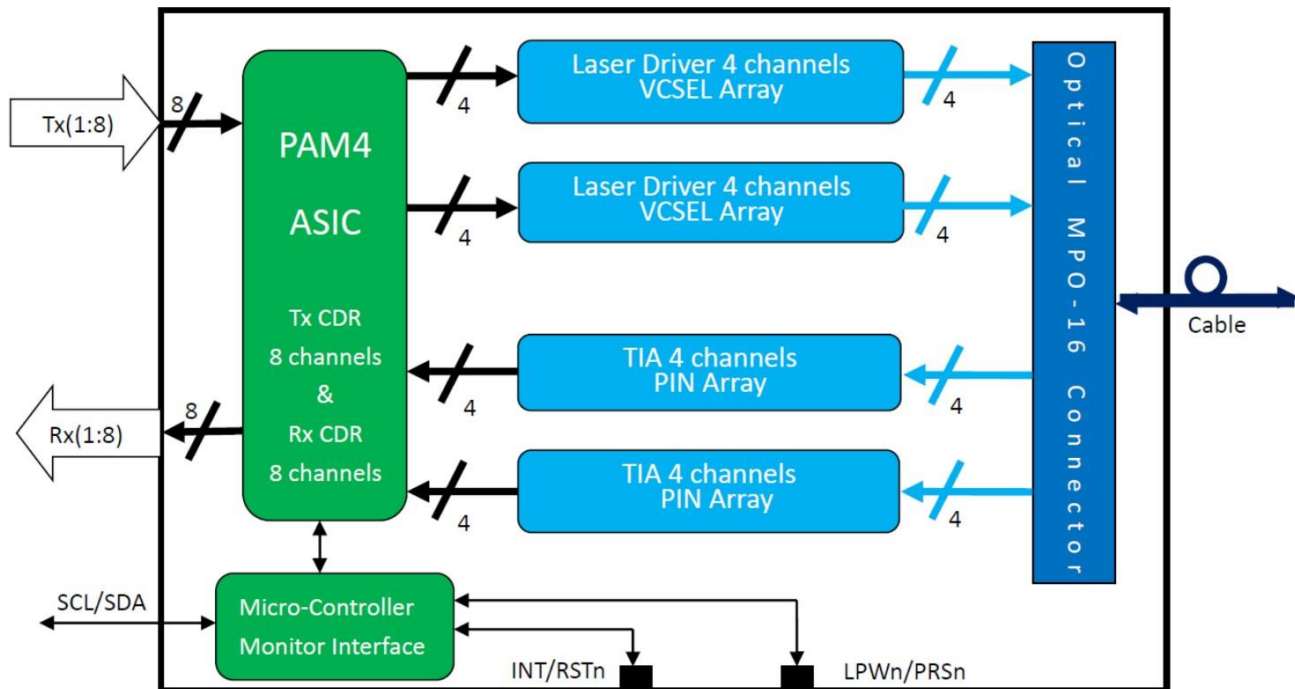


Figure 2. Block Diagram of One of the OSFP AOC End Modules

#### 4. Pin Assignment and Description

The electrical pinout of the OSFP module is shown in Figure 3 below.

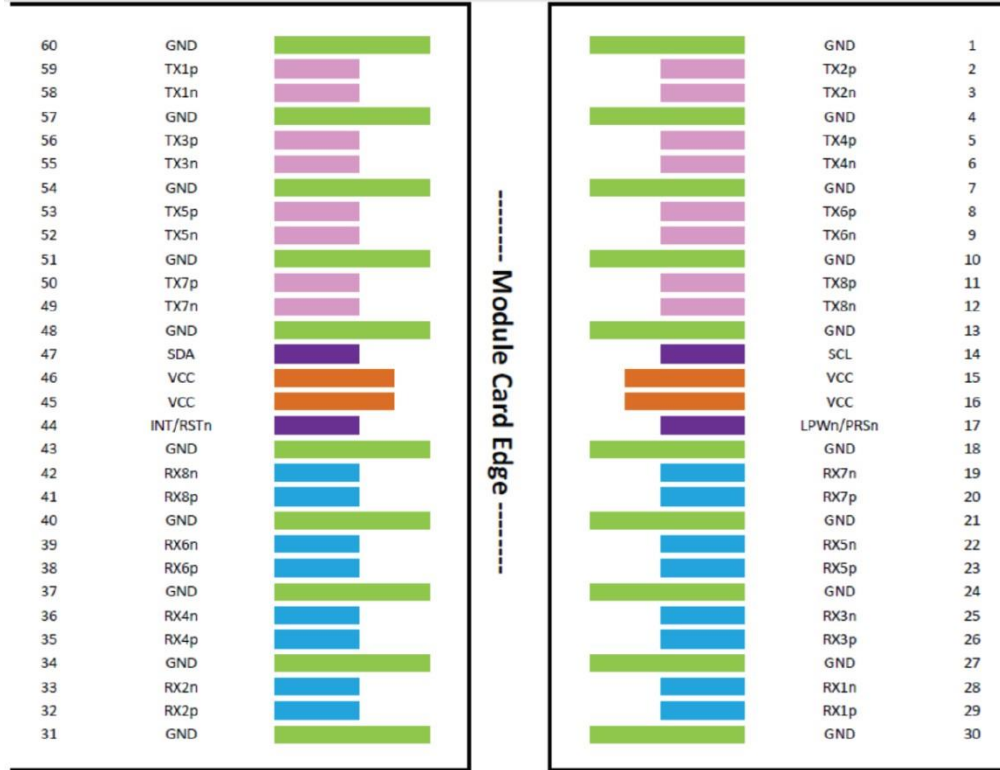


Figure 3. MSA Compliant Connector

#### Pin Definition

Pin#	Symbol	Description	Logic	Direction	Plug Sequence
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1

14	SCL	2-wire Serial interface clock	LVC MOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2



networks

47	SDA	2-wire Serial interface data	LVC MOS-I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3

\

50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
60	GND		Ground		1

### 5. Recommended Power Supply Filter

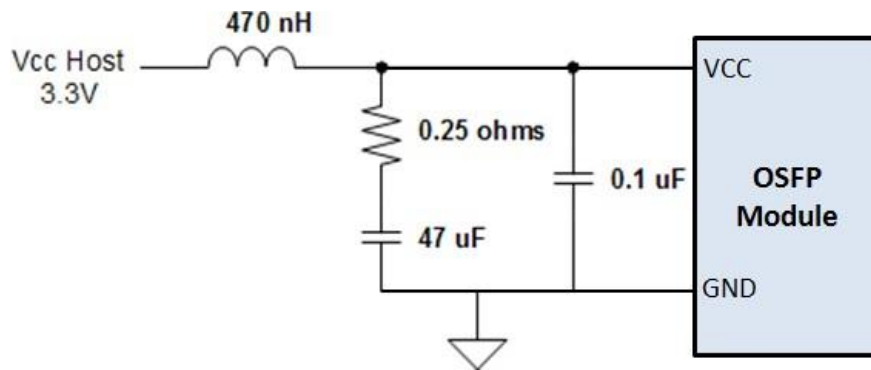


Figure 4. Recommended Power Supply Filter

### 6. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T <sub>s</sub>	-40	85	degC	
Operating Case Temperature	T <sub>OP</sub>	10	60	degC	
Power Supply Voltage	V <sub>CC</sub>	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	



## 7. Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T <sub>OP</sub>	20		60	degC	
Power Supply Voltage	V <sub>CC</sub>	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				2.4x10 <sup>-4</sup>		
Post-FEC Bit Error Ratio				1x10 <sup>-12</sup>		1
Link Distance with OM3	D	0.5		100	m	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

## 8. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				10	W	
Supply Current	I <sub>CC</sub>			3.03	A	
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	1
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance	TP1a	-0.4 to 3.3			V	

Range (Min)						
DC Common Mode Input Voltage	TP1	-350		2850	mV	3
<b>Receiver (each Lane)</b>						
Signaling Rate, each lane	TP4	26.5625 ± 100 ppm			GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

## 9. Mechanical Dimensions

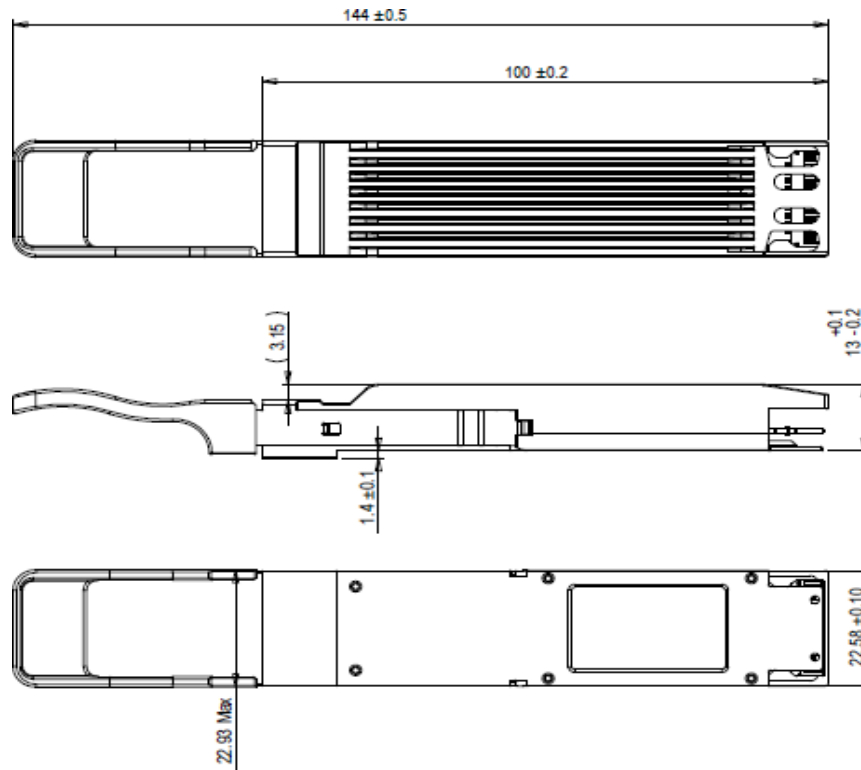


Figure 5. Mechanical Outline

## 10. ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

### **11. Laser Safety**

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.