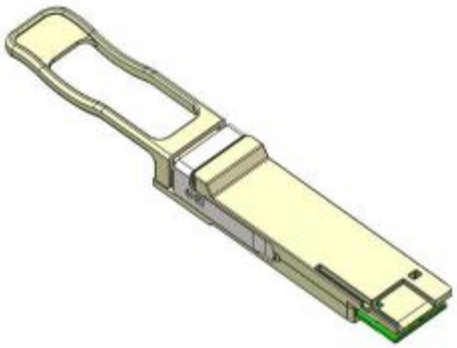

The 200G QSFP-DD SR8 Transceiver is designed to transmit and receive serial optical data links up to 28 Gb/s data rate(per channel) over multi-mode fiber. It is a small-form- factor hot pluggable transceiver module integrated with the high performance VCSEL laser and high sensitivity PIN receiver. It is compliant with 100G Ethernet specs; QSFP-DD MSA. It also functions as a 2x100G QSFP-DD SR8 transceiver that supports 2x100G connections to two 100G QSFP28 SR4 transceivers using a MPO breakout cable.

Features

- Up to 28Gbps data rate per channel
- 8 duplex channels transmitters and receivers
- Integrated 850nm VCSEL array and PD array
- Single MPO24 connector receptacle optical interface compliant
- Single +3.3V power supply
- DDM function implemented
- Hot-pluggable QSFP-DD form factor
- Maximum link length of 100m on 24 core MPO OM4 (MMF) fiber
- Power dissipation:<4.5W
- International class 1 laser safety certified
- Operating temperature range: 0℃ ~ +70 ℃
- Compliant with ROHS10

Applications

- 200GBASE-SR8 Ethernet
- 2×100GBASE-SR4 Ethernet
- Switch & Router Connections
- Data Centers
- Other 200G Interconnect Requirements.

Standards

- IEEE 802.3bm-2015
- QSFP-DD MSA
- CMIS 4.0

Specifications

(Tested under recommended operating conditions, unless otherwise noted)

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter(per Lane)						
Signaling Speed per Lane		Gbps		25.78125		NRZ
Center wavelength		nm	840	850	860	
RMS Spectral Width	SW	nm			0.6	
Average Launch Power per lane	TXPx	dBm	-8.4		2.4	
Tx OMA per lane	TxOMA	dBm	-6.4		3	
Difference in power between any two lane(OMA)	DPx	dBm			4	
Average launch power of off transmitter per lane		dBm			-30	
Transmitter and Dispersion eye closure per lane	TDEC	dB			4.3	
Launch power in OMA minus TDEC		dBm	-7.3			
Optical Extinction Ratio	ER	dB	2			
Optical Return Loss Tolerance	ORL	dB			12	
Encircled Flux	FLX	dBm	>86% at 19um			
			<30%at 4 5um			
Relative Intensity Noise	RIN	dB/Hz			-128	

Receiver(per Lane)						
Signaling Speed per Lane		Gbps		25.78125		NRZ
Center wavelength		nm	840		860	
Damage Threshold	DT	dBm	3 4			
Average receive power per lane	RXPx	dBm	-10.3		2.4	
Receiver power (OMA) per lane	RxOMA	dBm			3	
Receiver reflectance	Rfl	dB			-12	
vertical eye closure penalty，per lane		dB			1.9	
Stressed Receive Sensitivity(OMA) per lane	SRS	dBm			-5.2	
Sensitivity(OMA) per lane	S	dBm			-10.3	
LOS De-Assert	LOSD	dBm			-12	
LOS Assert	LOSA	dBm	-30			
LOS Hysteresis		dBm	5			

Ordering Information

Part No.	Specifications(per lane)									Application
	Package	Data rate	Laser	Optical Power	Detector	Sensitivity	Temp	Reach	Others	
200G-QDD-SR8	QSFP-DD	200G	850nm VCSEL	-8.4~2.4dBm	850nm PD	< -10.3dBm	0~70 °C	100m	RoHS	200G Base SR8

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	℃	-40	+85
Relative Humidity	RH	%	5	95
Power Supply Voltage	Vcc	V	-0.5	+3.6

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tc	°C	0	/	70
Power Supply Voltage	Vcc	V	3.14	3.3	3.46
NRZ Bit Rate(Per channel)	BR	Gbps		25.78	

Principle diagram

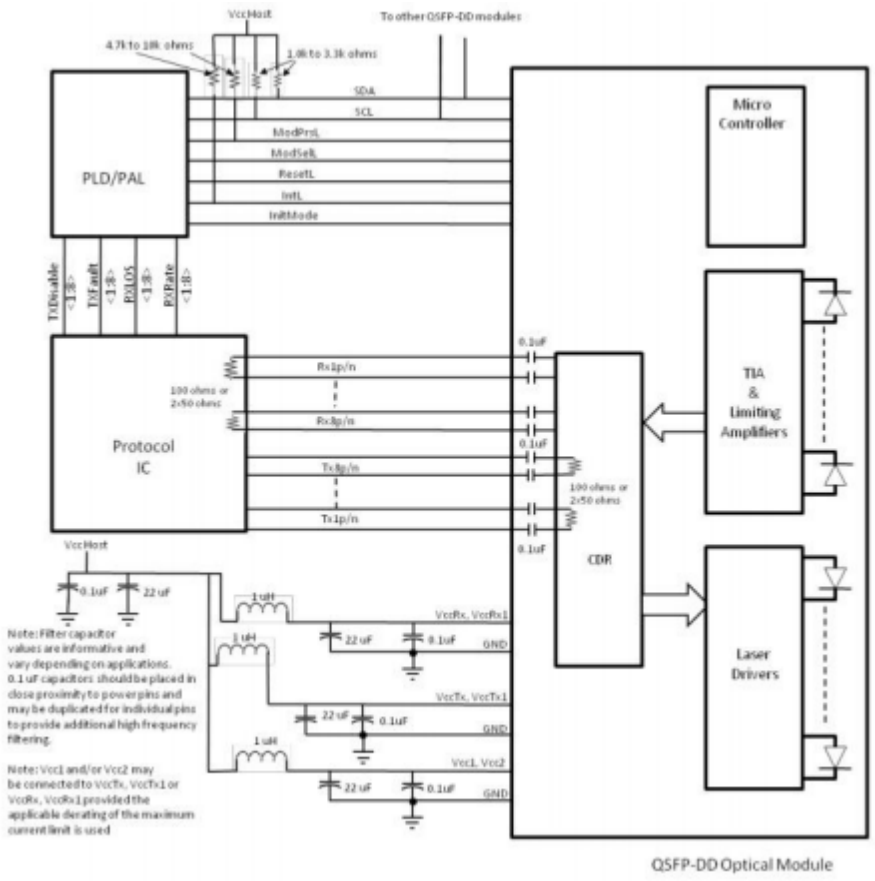

Figure 1. Module Principle Diagram

Electric Ports Definition

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Supply Voltage	VCC VCC3.3-Tx VCC3.3-Rx	V	3.14	3.3	3.46	
Supply Current	Icc	mA			1300	
Power Consumption	Pc	W			4.5	
Transceiver Power-on Initialize Time		ms			2000	
Transmitter						
Single Ended Input VoltageTolerance	VinT	V	-0.3		4.0	

Differential Data Input Swing	VIN	mVp-p	300		1200	
AC Common Mode Output Voltage(RMS)		mV	15			
Differential Input Impedance		Ω	90	100	110	
Receiver						
Single Ended Output Voltage	VoutR	V			0.2	
Differential Data Output Swing	Vout,PP	mVp-p	350		850	
AC Common Mode Output Voltage(RMS)		mV			7.5	
Differential Output Impedance		Ω	90	100	110	
IIC communication						
IIC Clock frequency	-	KHZ	/	100	400	
clock stretching	-	us	/	/	500	
Data hold time	-	ns	300	/	/	

Pin Description

PIN	Logic	Symbol	DESCRIPTION	NOTE
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCOMS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCOMS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-0	Rx3p	Receiver Non-Inverted Data Output	
15	CML-0	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-0	Rx1p	Receiver Non-Inverted Data Output	
18	CML-0	Rx1n	Receiver Inverted Data Output	

PIN	Logic	Symbol	DESCRIPTION	NOTE
19		GND	Ground	1
20		GND	Ground	1
21	CML-0	Rx2n	Receiver Inverted Data Output	
22	CML-0	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-0	Rx4n	Receiver Inverted Data Output	
25	CML-0	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-0	ModPrsL	Module Present	
28	LVTTL-0	IntL	Interrupt	
29		VccTx	+3 3 V Power Supply transmitter	2
30		Vcc1	+3 3 V Power Supply	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the IntiMode pad is called LPMode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		VccRx1	+3 3V Power Supply Receiver	2

PIN	Logic	Symbol	DESCRIPTION	NOTE
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-0	Rx7p	Receiver Non-Inverted Data Output	
53	CML-0	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-0	Rx5p	Receiver Non-Inverted Data Output	
56	CML-0	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-0	Rx6n	Receiver Inverted Data Output	
60	CML-0	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-0	Rx8n	Receiver Inverted Data Output	
63	CML-0	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	Not Connect	3
66		Reserved	For future use	3
67		VccTx 1	+3.3 V Power Supply transmitter	2
68		Vcc2	+3.3 V Power Supply	2
69		Reserved	For future use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

Notes:

1．QSFP-DD uses common ground (GND) for all signals and supply (power). All the common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connectedtheses directly to the host board signal common ground plane.

2．VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.

3．All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor Specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100pF.

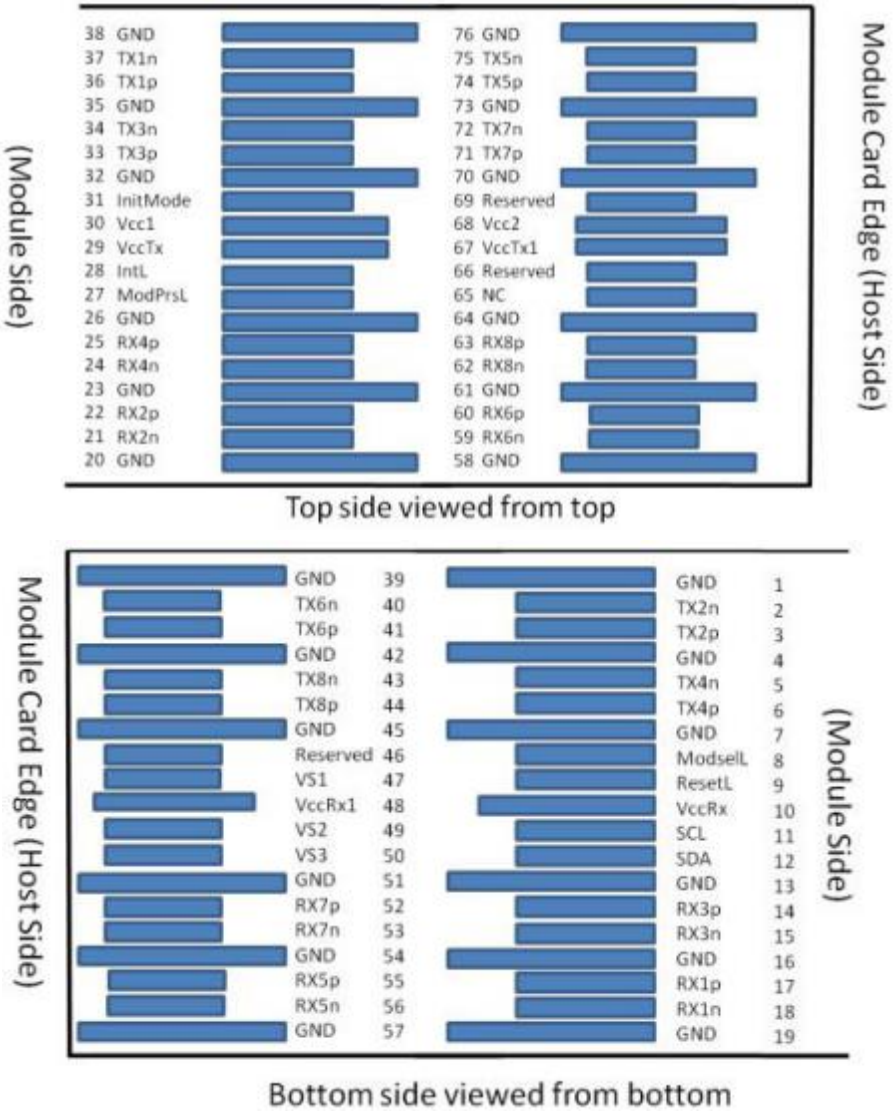

Figure 2. Electrical Pin-out Details

Digital Diagnostic Memory Map

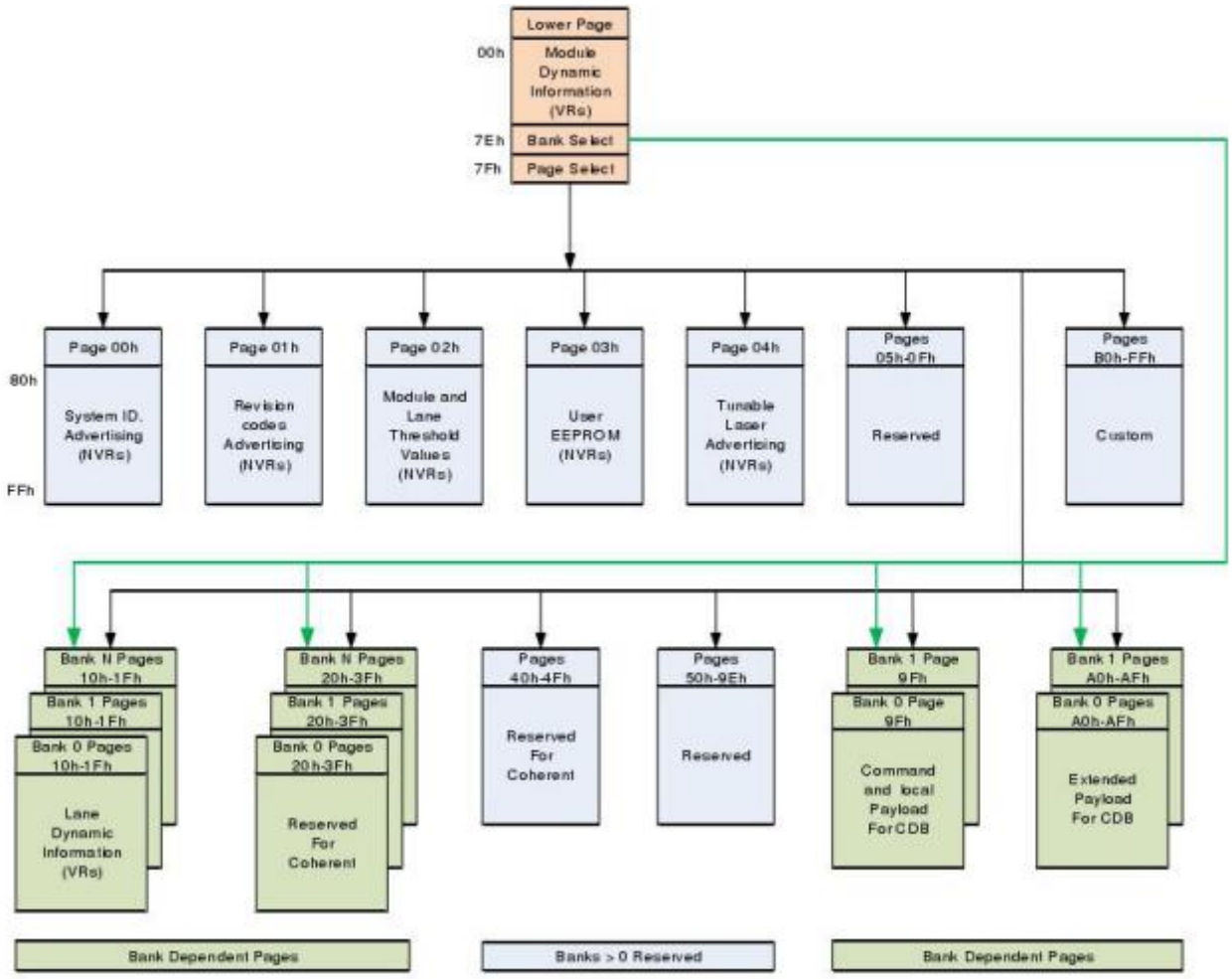

Figure 3 Digital Diagnostic Memory Map

Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Edge Card Connector. Figure is the suggested transceiver/host interface.

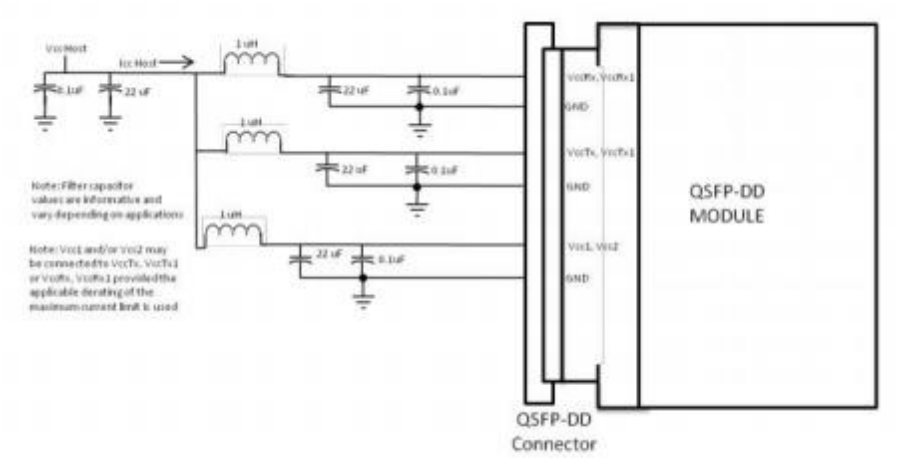

Figure 4 Recommended Host Board Power Supply Filtering

Module Mechanical Dimensions

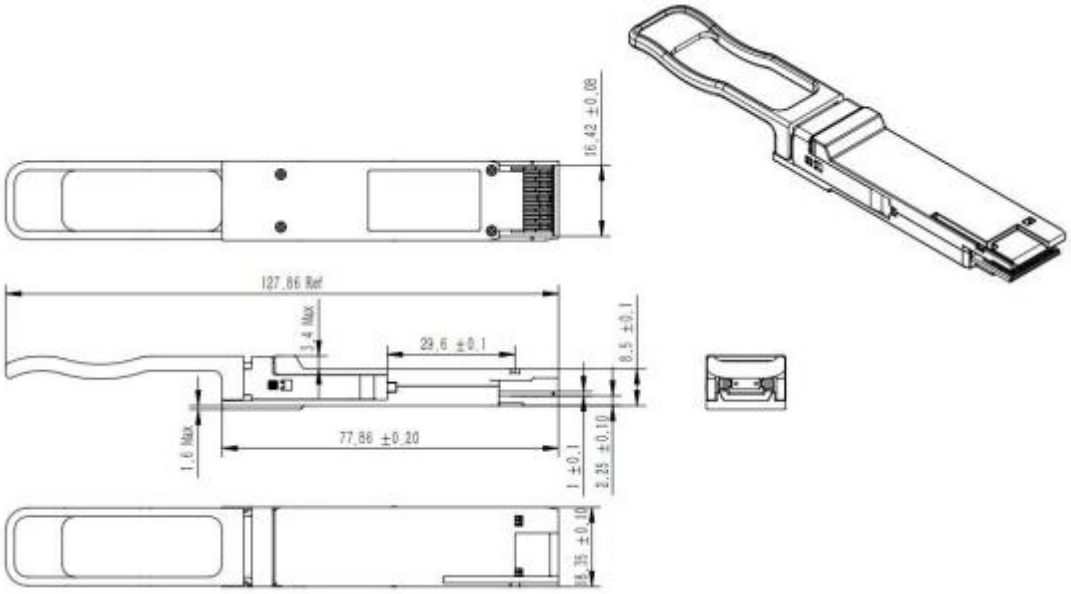

Figure 5 Package Outline

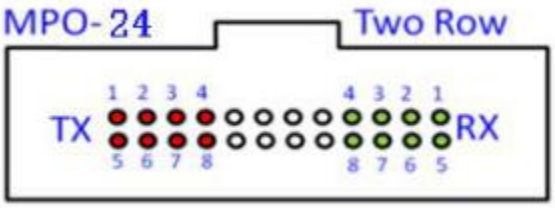

Figure 6 MPO Pinout Diagram and Description

Host PCB layout recommendation

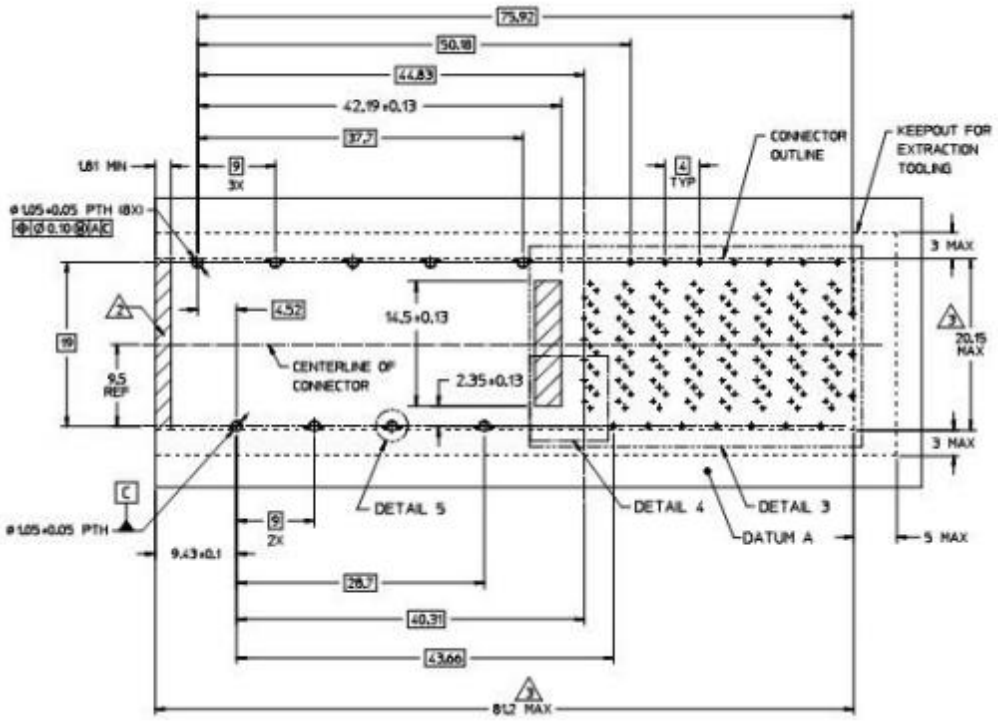

Figure 6 PCB Layout Recommendation