

400Gb/s OSFP PSM8 300m SMF Optical Transceiver

D-OP8FNH-H00

Product Specification

Features

- OSFP MSA compliant
- Silicon Photonic Basis
- 8 parallel lanes on 1550nm center wavelength
- Compliant to 400G_SiP_PSM8_Module Specification
- Up to 300m transmission on single mode fiber (SMF) with KP4 FEC
- Operating case temperature: 20 to 52°C
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Data Rate 53.125Gbps (PAM4) per channel.
- Maximum power consumption 9W
- MPO-16 connector
- RoHS compliant



Applications

- Data Center Interconnect
- 400G Ethernet
- Infiniband interconnects
- Enterprise networking

Part Number Ordering Information

| D-OP8FNH-H00 | 400G OSFP SiPh PSM8 300m SMF with FEC optical transceiver with full |
|--------------|---|
| | real-time digital diagnostic monitoring and pull tab |



1. General Description

This product is a parallel 400Gb/s Octal Small Form-factor Pluggable (OSFP) optical module. It provides increased port density and total system cost savings. The OSFP full-duplex optical module offers 8 independent transmit and receive channels, each capable of 53.125Gb/s operation for an aggregate data rate of 400Gb/s on 300m single mode fiber.

An optical fiber cable with an MTP/MPO-16 connector can be plugged into the OSFP PSM8 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through an OSFP MSA-compliant edge type connector.

It contains an optical MPO-16 connector for the optical interface and a 60-pin connector for the electrical interface. Host FEC is required to support up to 300m single mode fiber transmission.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the OSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

2. Functional Description

The module is silicon photonic basis. It incorporates 8 parallel channels, on 1550nm Center Wavelength, operating at 50G per channel. The transmitter uses a clock-and-data recovery (CDR) circuit, linear driver, and Silicon Mach-Zehnder modulator (MZM) with a 1550nm continuous wave (CW) laser as the optical source to generate a 26.5625Gbaud/s PAM4 optical signal. The receiver uses a Germanium (Ge) photodetector (PD), linear transimpedance amplifier (TIA), and CDR circuit to generate a 26.5625Gbaud/s PAM4 electrical signal to the host. The MZMs and PDs are integrated into a Silicon-based photonic integrated circuit (PIC). The electrical interface is compliant with IEEE 802.3bs and OSFP MSA in the transmitting and receiving directions, and the optical interface is compliant to OSFP MSA with MPO-16 Optical Connector. Figure 2 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up this product. As per MSA specifications the module offers 4 low speed hardware control pins: SCL, SDA, INT/RSTn and LPWn/PRSn

SCL and SDA are a 2-wire serial interface between the host and module using the I2C protocol. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value can be 2.2k ohms to 4.7k ohms.

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. Reset is an active-low signal on the host which is translated to an active-low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active-low signal on the host. The INT/RSTn signal operates in 3 voltage zones to indicate the



state of Reset for the module and Interrupt for the host. Figure 1 shows these 3 zones.

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host. The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 1 shows these 3 zones.



Figure 1. Voltage Zones



3. Transceiver Block Diagram



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4. Pin Assignment and Description

GND 60 GND 1 59 TX1p тх2р 2 58 TX1n TX2n 3 57 GND GND 4 56 ТХ3р TX4p 5 55 TX4n TX3n 6 54 GND GND 7 53 TX5p ТХ6р 8 52 TX5n TX6n 9 ---- Module Card Edge 51 GND GND 10 50 ТХ7р TX8p 11 49 TX7n TX8n 12 48 GND GND 13 47 SDA SCL 14 VCC VCC 15 46 45 VCC VCC 16 44 INT/RSTn LPWn/PRSn 17 43 GND GND 18 42 RX8n RX7n 19 41 RX8p 20 RX7p 40 GND GND 21 39 RX6n RX5n 22 1 38 RX5p 23 RX6p 37 GND GND 24 36 RX4n RX3n 25 35 26 RX4p RX3p 34 GND GND 27 RX1n 28 33 RX2n 32 RX2p RX1p 29 31 GND GND 30

The electrical pinout of the OSFP module is shown in Figure 3 below. Figure 4 shows the MPO-16 connector interface.

Figure 3. MSA Compliant Connector

| Pin Definition | | | | | | | |
|----------------|--------|-------------------------------|--------|-----------------|----------|--|--|
| Pin# | Symbol | Description | Logic | Direction | Plug | | |
| | | | | | Sequence | | |
| 1 | GND | | Ground | | 1 | | |
| 2 | ТХ2р | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | | |
| 3 | TX2n | Transmitter Data Inverted | CML-I | Input from Host | 3 | | |
| 4 | GND | | Ground | | 1 | | |
| 5 | ТХ4р | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | | |
| 6 | TX4n | Transmitter Data Inverted | CML-I | Input from Host | 3 | | |
| 7 | GND | | Ground | | 1 | | |
| 8 | ТХ6р | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 | | |
| 9 | TX6n | Transmitter Data Inverted | CML-I | Input from Host | 3 | | |
| 10 | GND | | Ground | | 1 | | |



| | TVO | Transmitten Data Nam Incontral | | In much fair and I have | 2 |
|----|-----------|------------------------------------|-------------|-------------------------|---|
| 11 | ТХ8р | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 12 | TX8n | Iransmitter Data Inverted | CML-I | Input from Host | 3 |
| 13 | GND | | Ground | | 1 |
| 14 | SCL | 2-wire Serial interface clock | LVCMOS- | Bi-directional | 3 |
| | | | 1/0 | | |
| 15 | NCC | | | Deven from the st | 2 |
| 15 | VCC | +3.3V Power | | Power from Host | 2 |
| 16 | | +3.3V Power | | Power from Host | 2 |
| 17 | LPWn/PRSn | Low-Power Mode / Module Present | Multi-Level | Bi-directional | 3 |
| 18 | GND | | Ground | | 1 |
| 19 | RX7n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 20 | RX7p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 21 | GND | | Ground | | 1 |
| 22 | RX5n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 23 | RX5p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 24 | GND | | Ground | | 1 |
| 25 | RX3n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 26 | RX3p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 27 | GND | | Ground | | 1 |
| 28 | RX1n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 29 | RX1p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 30 | GND | | Ground | | 1 |
| 31 | GND | | Ground | | 1 |
| 32 | RX2p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 33 | RX2n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 34 | GND | | Ground | | 1 |
| 35 | RX4p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 36 | RX4n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 37 | GND | | Ground | | 1 |
| 38 | RX6p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 39 | RX6n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 40 | GND | | Ground | | 1 |
| 41 | RX8p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 42 | RX8n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 43 | GND | | Ground | | 1 |
| 44 | INT/RSTn | Module Interrupt / Module Reset | Multi-Level | Bi-directional | 3 |
| 45 | VCC | +3.3V Power | | Power from Host | 2 |
| 46 | VCC | +3.3V Power | | Power from Host | 2 |
| | | | 1 | 1 | |



| 47 | SDA | 2-wire Serial interface data | LVCMOS- | Bi-directional | 3 |
|----|------|-------------------------------|---------|-----------------|---|
| | | | I/O | | |
| | | | | | |
| 48 | GND | | Ground | | 1 |
| 49 | TX7n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 50 | ТХ7р | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 51 | GND | | Ground | | 1 |
| 52 | TX5n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 53 | ТХ5р | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 54 | GND | | Ground | | 1 |
| 55 | TX3n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 56 | ТХ3р | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 57 | GND | | Ground | | 1 |
| 58 | TX1n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 59 | TX1p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 60 | GND | | Ground | | 1 |



Figure 4. MPO-16 Optical Connector Interface



5. Recommended Power Supply Filter



Figure 5. Recommended Power Supply Filter

6. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

| Parameter | Symbol | Min | Max | Units | Notes |
|--------------------------------------|-----------------|------|-----|-------|-------|
| Storage Temperature | Ts | -40 | 70 | degC | |
| Operating Case Temperature | T _{OP} | 20 | 52 | degC | |
| Power Supply Voltage | V _{CC} | -0.5 | 3.6 | V | |
| Relative Humidity (non-condensation) | RH | 0 | 85 | % | |

7. Recommended Operating Conditions and Power Supply Requirements

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|----------------------------|-----------------|-------|---------|----------------------|-------|-------|
| Operating Case Temperature | T _{OP} | 20 | | 52 | degC | |
| Power Supply Voltage | V _{CC} | 3.135 | 3.3 | 3.465 | V | |
| Data Rate, each Lane | | | 26.5625 | | GBd | PAM4 |
| Data Rate Accuracy | | -100 | | 100 | ppm | |
| Pre-FEC Bit Error Ratio | | | | 2.4x10 ⁻⁴ | | |
| Post-FEC Bit Error Ratio | | | | 1x10 ⁻¹² | | 1 |
| Link Distance | D | 0.5 | | 300 | m | 2 |

Notes:

- 1. FEC provided by host system.
- 2. FEC required on host system to support maximum distance.



8. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

| Parameter | Test Point | Min | Typical | Max | Units | Notes | | |
|--|------------|---|-------------|------|-------|-------|--|--|
| Power Consumption | | | | 9 | W | | | |
| Supply Current | Icc | | | 2.73 | А | | | |
| Transmitter (each Lane) | | | | | | | | |
| Differential Voltage Input Swing, pk-pk | TP1a | | | 900 | mVpp | | | |
| Differential Input Termination Resistance | TP1 | 90 | 100 | 110 | ohm | | | |
| DC Common Mode Input Voltage, | TP1 | -350 | | 2850 | mV | | | |
| Differential Input Return Loss | TP1 | ≥9.5-0.37 <i>f</i> , 0 ≥4.75-7.4log1 | lz ≦19Hz | dB | | | | |
| Differential to Common Mode Input Return Loss | TP1 | ≥22-(20/25.78) f, 0.01 ≤ f ≤ 12.89GHz ≥15-(6/25.78) f, 12.89 ≤ f ≤ 19GHz | | | dB | | | |
| | Receiv | ver (each Lane) | | | | | | |
| Differential Output Termination Resistance | TP4 | 90 | 100 | 110 | ohm | | | |
| Differential Voltage Output Swing, pk-pk | TP4 | | | 900 | mVpp | | | |
| AC Common Mode Output Voltage, RMS | TP4 | | | 17.5 | mV | | | |
| Differential Output Return Loss (SDD22) | TP4 | ≥9.5-0.37 <i>f</i> , 0.01 ≤ <i>f</i> ≤8GHz ≥4.75-7.4log10(<i>f</i> /14), 8≤ <i>f</i> ≤19Hz | | | dB | | | |
| Common Mode to Differential Return Loss | TP4 | ≥22-(20/25.78) f, 0.01 ≤ f ≤ 12.89GHz ≥15-(6/25.78) f, 12.89 ≤ f ≤ 19GHz | | | dB | | | |
| Vertical Eye Closure | TP4 | | | 5.8 | dB | | | |
| Eye Width | TP4 | 0.4 | | | UI | 1 | | |
| Eye Height(differential) | TP4 | 120 | | | mV | 1 | | |
| Common-Mode Output Return Loss | TP4 | 2 | | | dB | | | |

Notes:

1. Application to all three PAM4 eyes at BER level of 1E-6.



9. Optical Characteristics

| Parameter | Symbol | Min | Typical | Max | Units | Notes | | |
|--|-------------------|---|---------------|--------|-------|-----------|--|--|
| Transmitter | | | | | | | | |
| Center Wavelength | $\lambda_{\rm C}$ | 1544 | | 1558 | nm | | | |
| Data Rate, each Lane | | 26. | 5625 ± 100 p | pm | GBd | | | |
| Side Mode Suppression Ratio | SMSR | 35 | | | dB | Modulated | | |
| Outer Optical Modulation Amplitude (OMA _{outer}), each Lane | P _{OMA} | -3.3 | | 0 | dBm | | | |
| Launch Power in OMA _{outer} minus TDECQ, each Lane | | -3.8 | | | dB | | | |
| Difference in Average Launch Power Between Any Two Lanes | | | | 3 | dB | | | |
| Extinction Ratio | ER | 3 | | | dB | | | |
| Relative Intensity Noise | RIN | | | -135 | dB/Hz | | | |
| Transmitter Optical Mask | EMM | 25Gb/s: Compliant with 100GBASE-LR4 50Gb/s: TBD | | | % | | | |
| | 1 | Receive | r | r | r | ſ | | |
| Center Wavelength | $\lambda_{\rm C}$ | 1544 | | 1558 | nm | | | |
| Data Rate, each Lane | | 26. | .5625 ± 100 p | pm | GBd | | | |
| Receiver Saturation | | 3 | | | dBm | | | |
| Receiver Sensitivity (OMA _{outer}), each Lane | SEN1 | | | -6.3 | dBm | 1 | | |
| Receiver Sensitivity (OMA _{outer}), each Lane | SEN2 | | | -11.35 | dBm | 2 | | |
| Receiver Reflectance | R _R | | | -12 | dB | | | |
| LOS Assert | LOSA | | | -17 | dBm | OMA | | |
| LOS De-assert | LOSD | | | -16 | dBm | OMA | | |



Notes:

- 1. Tested with PRBS31 pattern at 53.13Gb/s, BER of 2E-4.
- 2. Tested with PRBS31 pattern at 25.78Gb/s, BER of 5E-5.

10. Digital Diagnostic Functions

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

| Parameter | Symbol | Min | Max | Units | Notes |
|--|--------------|------|-----|-------|----------------------------------|
| Temperature monitor absolute error | DMI_Temp | -3 | 3 | degC | Over operating temperature range |
| Supply voltage monitor absolute error | DMI_VCC | -0.1 | 0.1 | V | Over full operating range |
| Channel RX power monitor absolute error | DMI_RX_Ch | -2 | 2 | dB | 1 |
| Channel Bias current monitor | DMI_Ibias_Ch | -10% | 10% | mA | |
| Channel TX power monitor absolute error | DMI_TX_Ch | -2 | 2 | dB | 1 |

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.



11. Mechanical Dimensions





12. ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.



13. Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.