

D-OS4FNM-xxx

200Gb/s QSFP56 Active Optical Cable

DESCRIPTION

D-OS4FNM-xxx is a Four-Channel, Pluggable Active Optical Cable (AOC) for QSFP56 solution. The AOC integrate 4 independent transmit and receive channels, each capable of 26.56Gbd/s PAM4 operation for an aggregate data rate of 212.5Gb/s, which provides increased port density and total system cost savings for switches and routers, etc. Each end has a single QSFP56 connector for 200GbE application. It is compliant with IEEE 802.3bs, CMIS4.0 and QSFP MSA.

FEATURES

- 53.125Gb/s data rate per channel
- Available in standard lengths of 1, 3, 5, 7, 10, 15, 20, 30, 50m and 100m
- Typical power dissipation <5W per end
- Built-in digital diagnostic functions
- 850nm VCSEL transmitter
- BER less than 1E-6
- 3.3V power supply
- RoHS compliant
- Operating case temperature:0~+70°C

APPLICATION

The 200Gb/s QSFP56 active optical cable (AOC) can be used in the following applications:

- High-speed interconnects within/between switches, routers and transport equipment
- Server-server clusters



ABSOLUTE MAXIMUM RATINGS (TC=25°C, UNLESS OTHERWISE NOTED)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings will cause permanent damage and/or adversely affect device reliability.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	TS	-40	-	+70	°C	
Maximum Supply Voltage	Vcc	-0.3	-	3.6	V	
Operating Relative Humidity	RH	15	-	+85	%	

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Data Rate (per lane)	DR	-	53.125	-	Gb/s	
Pre-FEC Bit Error Rate	BER			1E-6		PRBS31Q
Operating Case temperature	Tc	0	-	+70	°C	
Supply Voltage	VCC	3.135	3.3	3.465	V	
Power Consumption		-	-	5	W	Per end
Data Speed Tolerance	ΔDR	-100	-	+100	ppm	

PIN Definitions

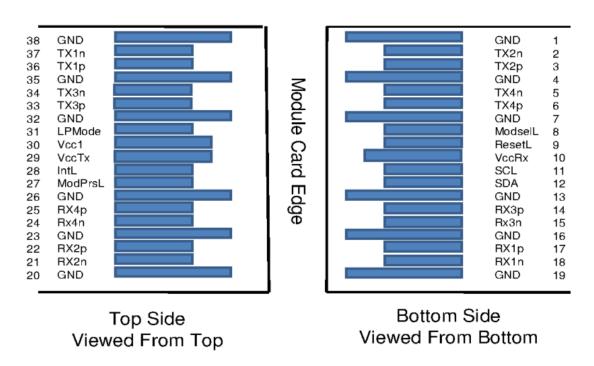


Figure 1 - Pin Definitions

PIN DESCRIPTIONS



Pin	Symbol	Name/Description	Ref.
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3 V Power supply receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	2
29	Vcc Tx	+3.3 V Power supply transmitter	
30	Vcc1	+3.3 V Power Supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Тх3р	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	



Pin	Symbol	Name/Description	Ref.
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes:

[1] Circuit ground is internally isolated from chassis ground.
[2] IntL is an open collector/drain output, which should be pulled up with a 4.7k – 10k Ohms resistor on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).



ELECTRICAL CHARACTERISTICS

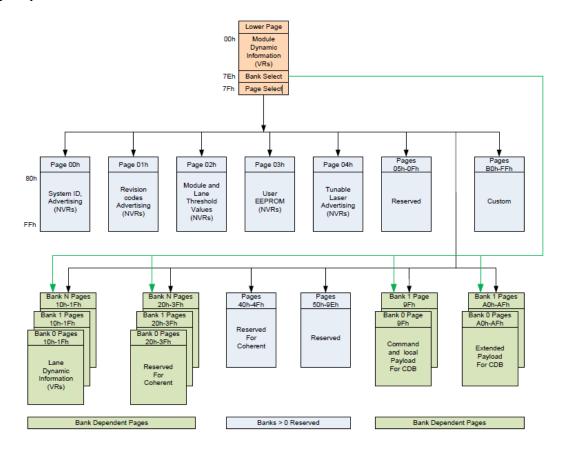
Parameter	Symbol	Min	Typical	Max	Units	Notes			
Receiver electrical output characteristics at TP4									
Signaling rate per lane			26.5625		GBd				
AC common-mode output voltage(RMS)			-	17.5	mV				
Differential peak-to-peak output voltage				900	mV				
Near-end ESMW (Eye symmetry mask width)			0.265		UI				
Near-end Eye height, differential		70			mV				
Far-end ESMW (Eye symmetry mask width)			0.2		UI				
Far-end Eye height, differential		30			mV				
Far-end pre-cursor ISI ratio		-4.5		2.5	%				
Differential output return loss		9.5 - 0.37f			dB	0.01 – 8 GHz			
Differential output return loss		4.75 -7.4log 10 (f/14)			dB	8 – 19 GHz			
Common to differential mode conversion return loss		22- 20(f/25.78)			dB	0.01 - 12.89 GHz			
conversion return loss		15 -6log 10 (f/25.78)			dB	12.89 – 19 GHz			
Differential termination mismatch				10	%				
Transition time (min, 20% to 80%)		9.5			ps				
DC common mode voltage		-350		2850	mV				
Transmitter electrical input chara	cteristics a	at TP1							
Signaling rate, per lane			26.5625		GBd				
Differential pk-pk input voltage tolerance		900			mV				
Differential input return loss		9.5 - 0.37f			dB	0.01 – 8 GHz			
Billoreritial inpat retain 1000		4.75 -7.4log 10 (f/14)			dB	8 – 19 GHz			
Differential to common mode input	ommon mode input	22-20(f/25.78)			dB	0.01 - 12.89 GHz			
return loss		15 -6log 10 (f/25.78)			dB	12.89 – 19 GHz			
Differential termination mismatch				10	%				
Module stressed input test		Per Section	120E.3.4.1	, IEEE802	2.3bs				
Single-ended voltage tolerance range		-0.4		3.3	V				
Common-mode voltage		-350		2850	mV				



LOW SPEED CONTROL AND SENSE SIGNALS

Parameter	Symbol	Min	Max	Unit	Notes/Conditions
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0 mA
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc + 0.5	V	
Capacitance on SCL and SDA I/O contact.	Ci		14	pF	Looking into the module SCL and SDA contacts.
Total bus capacitive load for SCL and SDA for up to 400 kHz SCL	Cb		100	рF	3.0 kΩ pullup resistor
rate (includes capacitance of all elements on the bus).			200	pF	1.6 kΩ pullup resistor
LPMode/TxDis, ResetL	VIL	-0.3	0.8	V	
and ModSelL	VIH	2	Vcc+0.3	V	
	Iin	-365	125	μΑ	0 V ≤ Vin ≤ Vcc
ModPrsL and	VOL	0	0.4	V	IOL=2.0mA
IntL/RxLOSL	VOH	Vcc-0.5	Vcc+0.3	V	

Memory Map





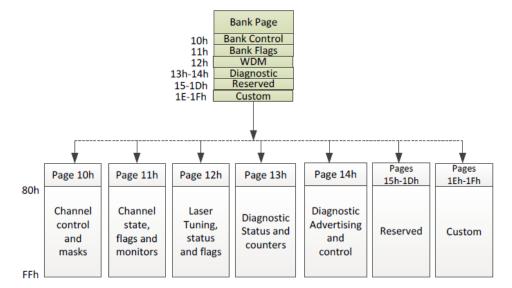


Figure 2 –QSFP56-Two-Wire Interface Fields

Page02 is User EEPROM and its format decided by user. The detail description of low memory and page00.page03 upper memory please see CMIS4.0 document.



DIGITAL DIAGNOSTIC SPECIFICATIONS

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transceiver Case Temperature	DMI_Temp	-3		+3	°C	Over operating temp
Supply voltage monitor absolute error	DMI_VCC	-3%		+3%	V	Full operating range
Channel RX power monitor absolute error	DMI_RX	-3		+3	dB	Per channel
Channel Bias current monitor	DMI_lbias	-10%		+10%	mA	Per channel
Channel TX power monitor absolute error	DMI_TX	-3		+3	dB	Per channel

OUTLINE DIAGRAM

unit: mm

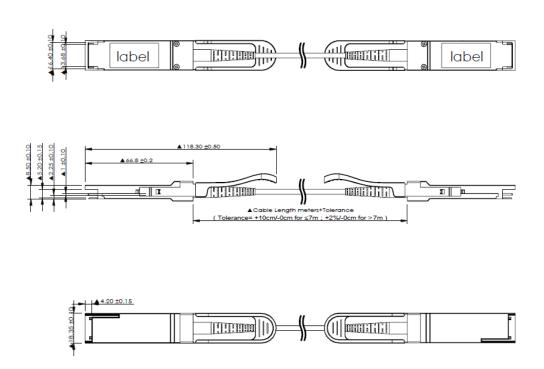


Figure 3 - Mechanical Dimensions



ESD SAFETY CAUTIONS

This transceiver is specified as ESD threshold 1KV for high speed data pins based on Human Body Model per ANSI/ESDA/JEDECJS-001. The units are subjected to 15kV air discharges during operation and 8kV direct contact discharges to the case. However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.