# 200Gb/s QSFP-DD LR4 10km Optical Transceiver

## D-DQ4FNL-N00

## Product Specification

**Features**

- IEEE802.3bs compliant
- QSFP-DD MSA compliant
- 4 LWDM lanes MUX/DEMUX design
- Supports 212.5Gb/s aggregate bit rate
- Up to 10km transmission on single mode fiber (SMF) with FEC
- Operating case temperature: 0 to 70°C
- 200GAUI-8 and 200GAUI-4 electrical interface
- Maximum power consumption 10.8W
- LC duplex connector
- RoHS compliant

**Applications**

- Data Center Interconnect
- 200G Ethernet
- Enterprise networking

**Part Number Ordering Information**

| | |
|---|---|
| **D-DQ4FNL-N00** | QSFP-DD LR4 10km with FEC optical transceiver with full real-time digital diagnostic monitoring and pull tab |

## 1. General Description

This product is a 200Gb/s transceiver module designed for 10km optical communication applications. The design is compliant to IEEE802.3bs 200GBASE-LR4 standard. For 200GAUI-8 Electrical interface, the module converts 8 input channels(ch) of 25Gb/s electrical data to 4 channels of LWDM optical signals, and multiplexes them into a single channel for 200Gb/s (PAM4) optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 200Gb/s(PAM4) input into 4 LWDM channels of signals, and converts them to 8 channels output electrical data . For 200GAUI-4 Electrical interface, the module converts 4 input channels(ch) of 50Gb/s electrical data to 4 channels of LWDM optical signals, and multiplexes them into a single channel for 200Gb/s (PAM4) optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 200Gb/s(PAM4) input into 4 LWDM channels of signals, and converts them to 4 channels output electrical data .

The central wavelengths of the 4 LWDM channels. It contains a duplex LC connector for the optical interface and a 76-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module. Host FEC is required to support up to 10km fiber transmission.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

## 2. Functional Description

This product converts the 8-channel of 25Gb/s or 4-channel of 50Gb/s electrical input data into LWDM optical signals .The transmitter path incorporates a quad channel EML driver and EML lasers together with an optical multiplexer. The light is combined by the MUX parts as a 200Gb/s data, propagating out of the transmitter module from the SMF. On the receiver path, an optical de-multiplexer is coupled to a 4 channel photodiode array. A DSP basis gearbox is used to convert 8 channels of 25GBaud PAM4 signals into 4 channels or 8 channels of 25GBaud NRZ signals and also an 8-channel retimer and FEC block are integrated in this DSP. The electrical interface is compliant with IEEE 802.3bs and QSFP-DD MSA in the transmitting and receiving directions, and the optical interface is compliant to IEEE 802.3bs with duplex LC connector.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2- wire serial communication commands. The ModSelL allows the use of this product on a single 2-

wire interface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP+ memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

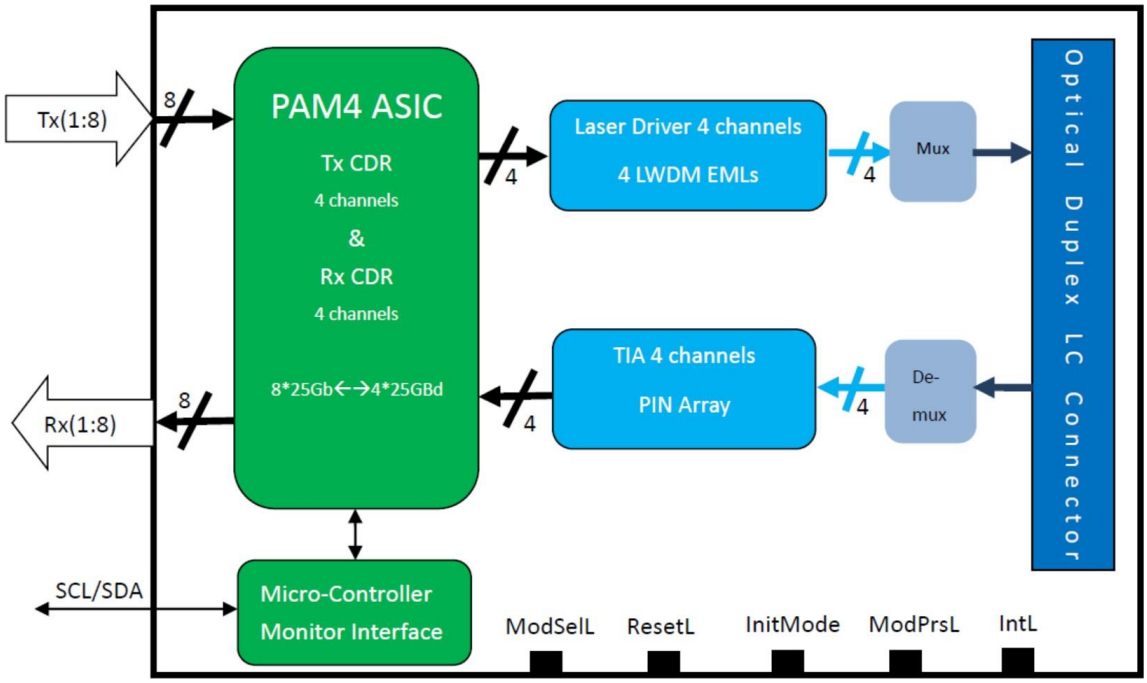
Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a "Low" state.

Interrupt (IntL) is an output pin. "Low" indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

## 3. Transceiver Block Diagram

**For 200GAUI-8**




**For 200GAUI-4**

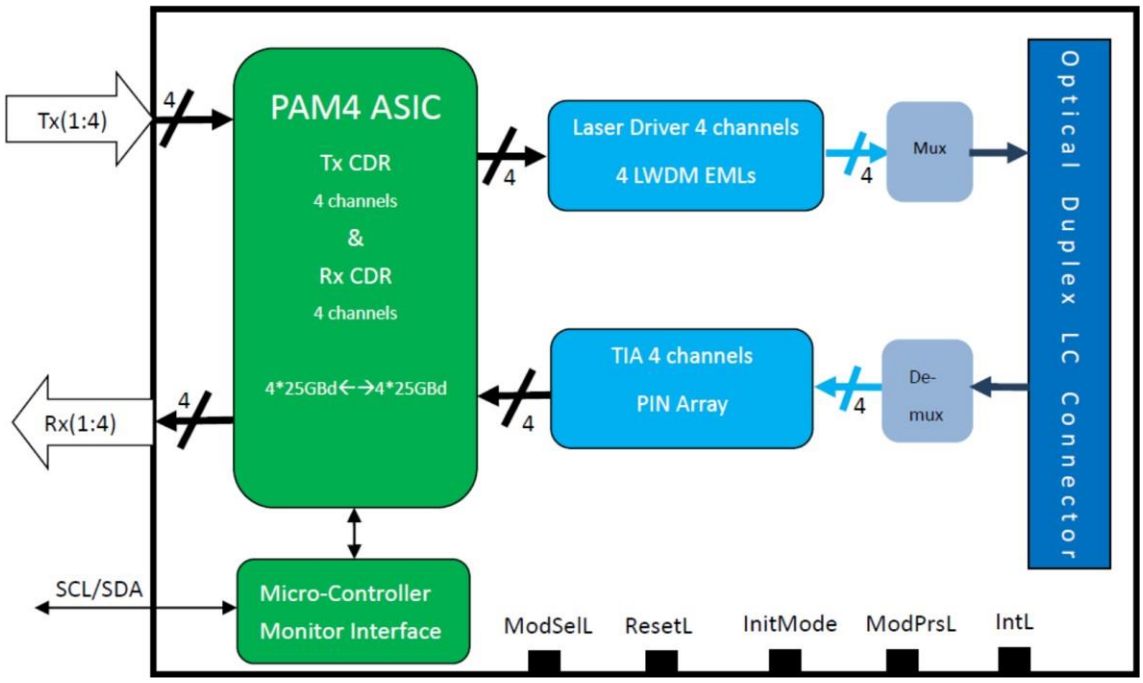



**Figure 1. Transceiver Block Diagram**

## 4. Pin Assignment and Description

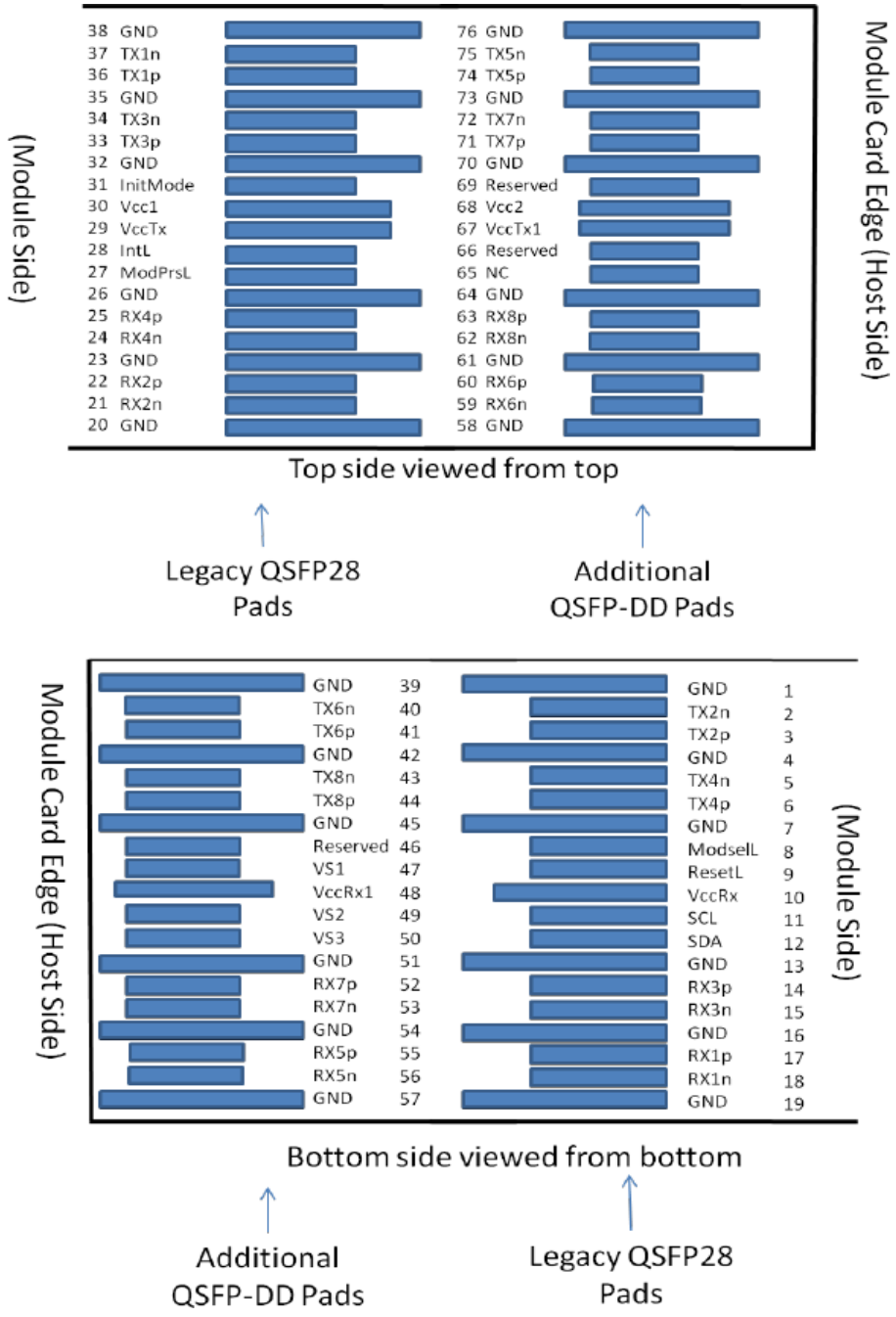



**Figure 2. MSA compliant Connector**

networks

**Pin Definition**

| Pin # | Logic | Symbol | Description | Plug Sequence | Notes |
|---|---|---|---|---|---|
| 1 | | GND | Ground | 1B | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | 3B | |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input | 3B | |
| 4 | | GND | Ground | 1B | 1 |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input | 3B | |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input | 3B | |
| 7 | | GND | Ground | 1B | 1 |
| 8 | LVTTL-I | ModSelL | Module Select | 3B | |
| 9 | LVTTL-I | ResetL | Module Reset | 3B | |
| 10 | | VccRx | +3.3V Power Supply Receiver | 2B | 2 |
| 11 | LVCMOS-I/O | SCL | 2-wire serial interface clock | 3B | |
| 12 | LVCMOS-I/O | SDA | 2-wire serial interface data | 3B | |
| 13 | | GND | Ground | 1B | 1 |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output | 3B | |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output | 3B | |
| 16 | GND | Ground | 1B | | 1 |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | 3B | |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | 3B | |
| 19 | | GND | Ground | 1B | 1 |
| 20 | | GND | Ground | 1B | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | 3B | |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | 3B | |
| 23 | | GND | Ground | 1B | 1 |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | 3B | |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | 3B | |
| 26 | | GND | Ground | 1B | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present | 3B | |
| 28 | LVTTL-O | IntL | Interrupt | 3B | |
| 29 | | VccTx | +3.3V Power supply transmitter | 2B | 2 |
| 30 | | Vcc1 | +3.3V Power supply | 2B | 2 |
| 31 | LVTTL-I | InitMode | Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE | 3B | |
| 32 | | GND | Ground | 1B | 1 |
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input | 3B | |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input | 3B | |
| 35 | | GND | Ground | 1B | 1 |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input | 3B | |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input | 3B | |
| 38 | | GND | Ground | 1B | 1 |

| | | | | | |
|---|---|---|---|---|---|
| 39 | | GND | Ground | 1A | 1 |
| 40 | CML-I | Tx6n | Transmitter Inverted Data Input | 3A | |
| 41 | CML-I | Tx6p | Transmitter Non-Inverted Data Input | 3A | |
| 42 | | GND | Ground | 1A | 1 |
| 43 | CML-I | Tx8n | Transmitter Inverted Data Input | 3A | |
| 44 | CML-I | Tx8p | Transmitter Non-Inverted Data Input | 3A | |
| 45 | | GND | Ground | 1A | 1 |
| 46 | | Reserved | For future use | 3A | 3 |
| 47 | | VS1 | Module Vendor Specific 1 | 3A | 3 |
| 48 | | VccRx1 | 3.3V Power Supply | 2A | 2 |
| 49 | | VS2 | Module Vendor Specific 2 | 3A | 3 |
| 50 | | VS3 | Module Vendor Specific 3 | 3A | 3 |
| 51 | | GND | Ground | 1A | 1 |
| 52 | CML-O | Rx7p | Receiver Non-Inverted Data Output | 3A | |
| 53 | CML-O | Rx7n | Receiver Inverted Data Output | 3A | |
| 54 | | GND | Ground | 1A | 1 |
| 55 | CML-O | Rx5p | Receiver Non-Inverted Data Output | 3A | |
| 56 | CML-O | Rx5n | Receiver Inverted Data Output | 3A | |
| 57 | | GND | Ground | 1A | 1 |
| 58 | | GND | Ground | 1A | 1 |
| 59 | CML-O | Rx6n | Receiver Inverted Data Output | 3A | |
| 60 | CML-O | Rx6p | Receiver Non-Inverted Data Output | 3A | |
| 61 | | GND | Ground | 1A | 1 |
| 62 | CML-O | Rx8n | Receiver Inverted Data Output | 3A | |
| 63 | CML-O | Rx8p | Receiver Non-Inverted Data Output | 3A | |
| 64 | | GND | Ground | 1A | 1 |
| 65 | | NC | No Connect | 3A | 3 |
| 66 | | Reserved | For future use | 3A | 3 |
| 67 | | VccTx1 | 3.3V Power Supply | 2A | 2 |
| 68 | | Vcc2 | 3.3V Power Supply | 2A | 2 |
| 69 | | Reserved | For Future Use | 3A | 3 |
| 70 | | GND | Ground | 1A | 1 |
| 71 | CML-I | Tx7p | Transmitter Non-Inverted Data Input | 3A | |
| 72 | CML-I | Tx7n | Transmitter Inverted Data Input | 3A | |
| 73 | | GND | Ground | 1A | 1 |
| 74 | CML-I | Tx5p | Transmitter Non-Inverted Data Input | 3A | |
| 75 | CML-I | Tx5n | Transmitter Inverted Data Input | 3A | |
| 76 | | GND | Ground | 1A | 1 |

Notes:

1. GND is the symbol for signal and supply (power) common for QSFP-DD modules. All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common

ground plane.

2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 3 below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP-DD transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

## 5. Recommended Power Supply Filter

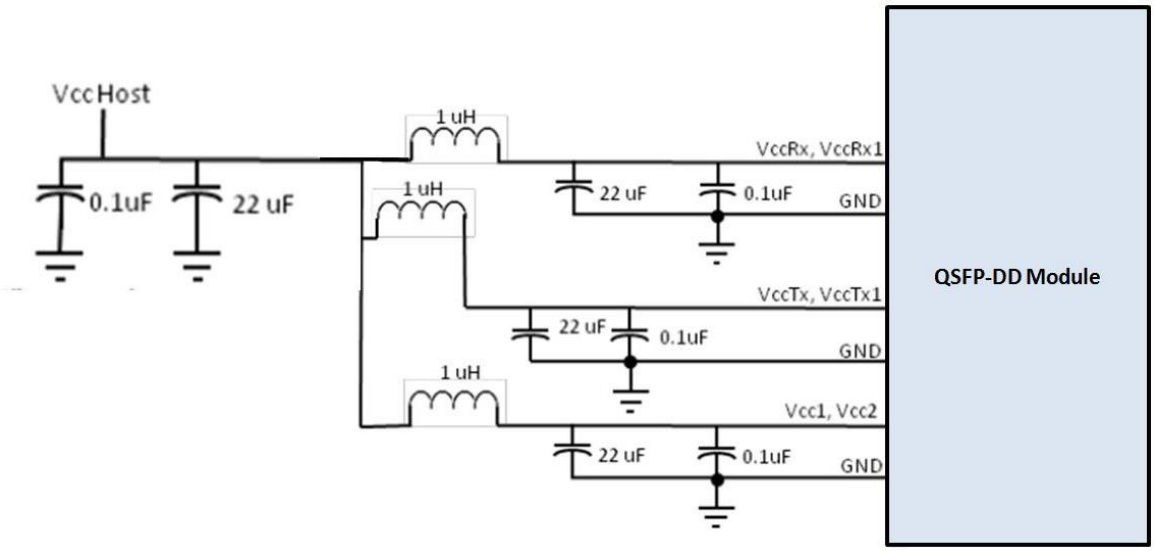



**Figure 3. Recommended Power Supply Filter**

## 6. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | -40 | 85 | degC | |
| Operating Case Temperature | $T_{OP}$ | 0 | 70 | degC | |
| Power Supply Voltage | $V_{CC}$ | -0.5 | 3.6 | V | |
| Relative Humidity (non-condensation) | RH | 0 | 85 | % | |
| Damage Threshold, each Lane | $TH_d$ | 3.5 | | dBm | |

## 7. Recommended Operating Conditions and Power Supply Requirements

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Operating Case Temperature | $T_{OP}$ | 0 | | 70 | degC | |
| Power Supply Voltage | $V_{CC}$ | 3.135 | 3.3 | 3.465 | V | |
| Data Rate, each Lane | | | 26.5625 | | GBd | |
| | | | 53.125 | | Gb/s | |
| Data Rate Accuracy | | -100 | | 100 | ppm | |
| Pre-FEC Bit Error Ratio | | | | $2.4x10^{-4}$ | | |
| Post-FEC Bit Error Ratio | | | | $1x10^{-12}$ | | 1 |
| Control Input Voltage High | | 2 | | Vcc | V | |
| Control Input Voltage Low | | 0 | | 0.8 | V | |
| Link Distance with G.652 | D | 0.002 | | 10 | km | 2 |

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

**8. Electrical Characteristics**

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

**200GAUI-8 Electrical Characteristics**

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Power Consumption | | | | 10.8 | W | |
| Supply Current | Icc | | | 3258 | mA | |
| Transmitter (each Lane) | | | | | | |
| Signaling rate per lane(200GBASE-LR4) | | 26.5625±100ppm | | | GBd | |
| Peak-to-peak differential output voltage | | | | 900 | mv | |
| AC common-mode output voltage | | 17.5 mV RMS with respect to signal ground | | | mV | |
| Differential output return loss | | Meets Equation (120D-2) constraints | | | | |
| Reference impedance for output return loss | | 100 | | | Ω | |
| Common to differential mode conversion | Zin | Meets Equation (83E–3) constraints | | | | |
| Differential termination mismatch | | Less than 10% | | | | |
| Transition time | | Greater than or equal to 12 ps | | | | |
| Eye width | | 0.57 | | | UI | |
| Eye height | | 228 | | | mV | |
| Crosstalk source | | Asynchronous crosstalk | | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | source using Pattern 5, Pattern 3, or valid 200GBASE-R signal | | | | |
| Vertical eye closure | | | | 5.5 | dB | |
| Receiver (each Lane) | | | | | | |
| Single-ended Output Voltage | | -0.4 | | 3.3 | V | Referred to signal common |
| Differential pk-pk input voltage tolerance | | 900 | | | mV | |
| Differential input return loss | | Equation (83E–5) | | | | |
| Differential to common-mode input returnloss | | Equation (83E–6) | | | | |
| Termination Mismatch at 1MHz | | | | 10 | % | |
| Module stressed input test | | See 83E.3.4.1 | | | | |
| DC common mode voltage | | -350 | | 2850 | mv | |
| Eye width | | 0.46 | | | UI | |
| Eye height | | 95 | | | mV | |

**200GAUI-4 Electrical Characteristics**

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Power Consumption | | | | 10.8 | W | |
| Supply Current | Icc | | | 3258 | mA | |

| Transmitter (each Lane) | | | | | | |
|---|---|---|---|---|---|---|
| Signaling rate per lane(200GBASE-LR4) | | 26.5625±100ppm | | | GBd | |
| Peak-to-peak differential output voltage | | | | 900 | mv | |
| AC common-mode output voltage | | | | 17.5 | mV | |
| Differential output return loss | | Equation (83E-2) | | | | |
| Common to differential mode conversion | Zin | Equation (83E–3) | | | | |
| Differential termination mismatch | | | | 10 | % | |
| Transition time (20% to 80%) | | 9.5 | | | ps | |
| DC common mode voltage | | -350 | | 2850 | mV | |
| Receiver (each Lane) | | | | | | |
| Single-ended Output Voltage | | -0.4 | | 3.3 | V | Referred to signal common |
| Differential pk-pk input voltage tolerance | | 900 | | | mV | |
| Differential input return loss | | Equation (83E–5) | | | | |
| Differential to common-mode input returnloss | | Equation (83E– | | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | 6) | | | | |
| Termination Mismatch at 1MHz | | | | 10 | % | |
| Module stressed input test | | See 120E.3.4.1 | | | | |
| DC common mode voltage | | -350 | | 2850 | mv | |

**9. Optical Characteristics**

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Wavelength Assignment | L0 | 1294.53 | 1295.56 | 1296.59 | nm | |
| | L1 | 1299.02 | 1300.05 | 1301.09 | nm | |
| | L2 | 1303.54 | 1304.58 | 1305.63 | nm | |
| | L3 | 1308.09 | 1309.14 | 1310.19 | nm | |
| **Transmitter** | | | | | | |
| Data Rate, each Lane | | 26.5625 ± 100 ppm | | | GBd | |
| Modulation Format | | PAM4 | | | | |
| Side-mode Suppression Ratio | SMSR | 30 | | | dB | Modulated |
| Total Average Launch Power | $P_T$ | | | 11.3 | dBm | |
| Average Launch Power, each Lane | $P_{AVG}$ | -3.4 | | 5.3 | dBm | 1 |
| Outer Optical Modulation Amplitude ($OMA_{outer}$), each Lane | $P_{OMA}$ | -0.4 | | 5.1 | dBm | 2 |
| Launch Power in $OMA_{outer}$ minus TDECQ, each Lane | | -1.8 | | | dB | For ER ≥4.5dB |
| | | -1.7 | | | dB | For ER <4.5dB |
| Transmitter and Dispersion Eye Clouser for PAM4, each Lane | TDECQ | | | 3.4 | dB | |
| Extinction Ratio | ER | 3.5 | | | dB | |
| Difference in Launch Power between any Two Lanes ($OMA_{outer}$) | | | | 4 | dB | |

| | | | | | | |
|---|---|---|---|---|---|---|
| $RIN_{16.5}OMA$ | RIN | | | -132 | dB/Hz | |
| Optical Return Loss Tolerance | TOL | | | 15.1 | dB | |
| Transmitter Reflectance | $T_R$ | | | -26 | dB | |
| Average Launch Power of OFF Transmitter, each Lane | $P_{off}$ | | | -30 | dBm | |
| **Receiver** | | | | | | |
| Data Rate, each Lane | | 26.5625 ± 100 ppm | | | GBd | |
| Modulation Format | | PAM4 | | | | |
| Damage Threshold, each Lane | $TH_d$ | 6.3 | | | dBm | 3 |
| Average Receive Power, each Lane | | -9.7 | | 5.3 | dBm | 4 |
| Receive Power ($OMA_{outer}$), each Lane | | | | 5.1 | dBm | |
| Difference in Receiver Power between any Two Lanes ($OMA_{outer}$) | | | | 4.2 | dB | |
| Receiver Sensitivity ($OMA_{outer}$), each Lane | SEN | | | -7.7 | dBm | For BER of 2.4E-4 |
| Stressed Receiver Sensitivity ($OMA_{outer}$), each Lane | SRS | | | -5.2 | dBm | 5 |
| Receiver Reflectance | $R_R$ | | | -26 | dB | |
| LOS Assert | LOSA | -25.7 | | | dBm | |
| LOS De-assert | LOSD | | | -11.7 | dBm | |
| LOS Hysteresis | LOSH | 0.5 | | | dB | |
| Stressed Conditions for Stress Receiver Sensitivity (Note 6) | | | | | | |
| Stressed Eye Closure for PAM4 (SECQ), Lane under Test | | | | 3.4 | dB | |
| $OMA_{outer}$ of each Aggressor Lane | | | -1 | | dBm | |

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 4.5 dB, the $OMA_{outer}$ (min) must exceed the minimum value specified here.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Measured with conformance test signal for BER = $2.4x10^{-4}$.
6. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

**10. Digital Diagnostic Functions**

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Temperature monitor absolute error | DMI_Temp | -3 | 3 | degC | Over operating temperature range |
| Supply voltage monitor absolute error | DMI _VCC | -0.1 | 0.1 | V | Over full operating range |
| Channel RX power monitor absolute error | DMI_RX_Ch | -3 | 3 | dB | |
| Channel Bias current monitor | DMI_Ibias_Ch | -10% | 10% | mA | |
| Channel TX power monitor absolute error | DMI_TX_Ch | -3 | 3 | dB | |

## 11. Mechanical Dimensions

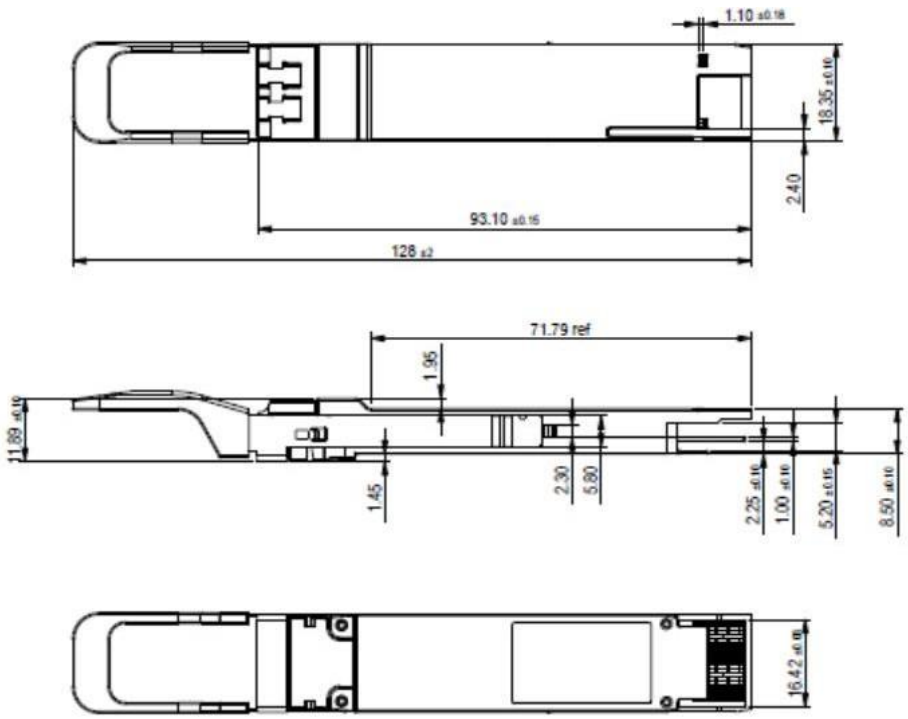



**Figure 4. Mechanical Outline**

## 12. ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

## 13. Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.