80km 100GBASE-ZR4 CFP2 Optical Transceiver Module

PRODUCT FEATURES

- CFP2 MSA compliant
- Digital diagnostic monitoring support
- Hot pluggable 104 pin electrical interface
- 4 LAN-WDM lanes MUX/DEMUX design
- 4x25G electrical interface
- Maximum power consumption 12W
- LC duplex connector
- Supports 103.125Gb/s bit rate
- Up to 80km transmission on single mode fiber
- Operating case temperature: 0℃ to 70℃
- Single 3.3V power supply
- RoHS 2.0 compliant

APPLICATIONS

- 100GBASE-ZR4 100G Ethernet
- Telecom networking
- Data Center Interconnect

DESCRIPTIONS

The module are designed for 80km optical communication applications. This module contains 4-lane optical transmitter, 4-lane optical receiver and the optical signals are multiplexed to a single-

mode fiber through an industry standard LC connector. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via MDIO interface. A block diagram is shown in Figure 1.

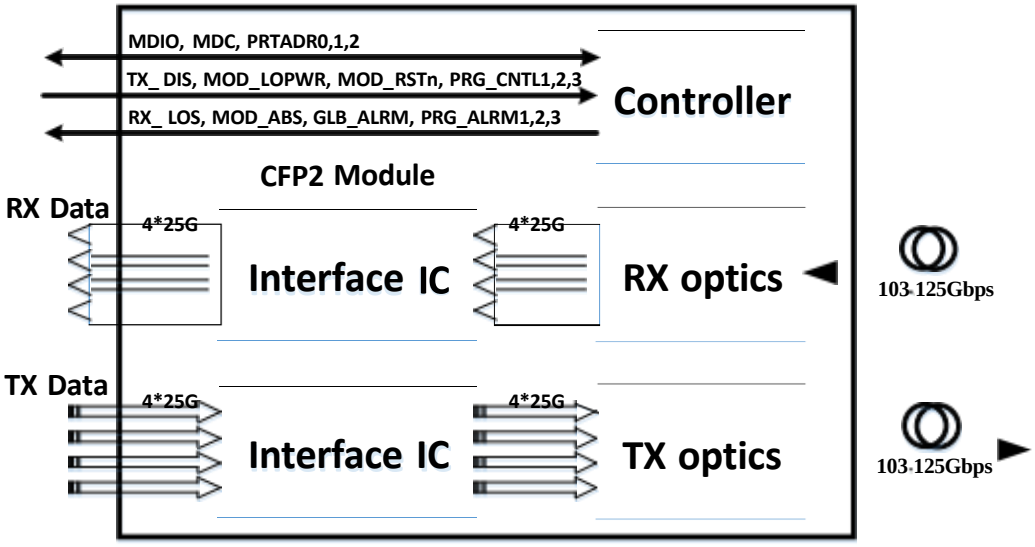

Figure 1. Transceiver Block Diagram

PRG_CNTL1:

Programmable Control Pin 1 (PRG_CNTL1) is an input pin from the Host, operating with programmable logic . It is pulled up in the CFP2 module. It can be re-programmed over MDIO registers to another MDIO control register while the module is in any steady state except Reset. The CFP2 MSA specifies that the default function be Transmit & Receive circuitry reset (TRXIC_RSTn) with active-low logic. When TRXIC_RSTn is asserted (driven low) the digital transmit and receive circuitry is reset clearing all FIFOs and/or resetting all CDRs and/or DLLs. When de-asserted, the digital transmit and receive circuitry resumes normal operation.

PRG_CNTL2:

Programmable Control Pin 2 (PRG_CNTL2) is an input pin from the Host, operating with programmable logic . It is pulled up in the CFP2 module. It can be re-programmed over MDIO registers to another MDIO control register while the module is in any steady state except Reset. The CFP2 MSA specifies that the default function be least significant bit of a two-bit code for Hardware Interlock.

PRG_CNTL3:

Programmable Control Pin 3 (PRG_CNTL3) is an input pin from the Host, operating with programmable logic . It is pulled up in the CFP2 module. It can be re-programmed over MDIO registers to another MDIO

control register while the module is in any steady state except Reset. The CFP2 MSA specifies that the default function be the most siginificant bit of a two-bit code for Connector Power Rating. Together with the Programmable Control Pin 2, the host uses this Code as the Hardware Interlock to inform what the power rating is supported by host at the connector.

TX_Diable:

TX Disable Pin (TX_DIS) is an input pin from the Host, operating with active-high logic. This pin is pulled up in the CFP2. When TX_DIS is asserted, all of the optical outputs inside a CFP2 module shall be turned off. When this pin is de-asserted, transmitters in a CFP2 module shall be turned on according to a predefined TX turned-on process. A maximum time is defined for the transmitter turn-on process. This time is vendor and/or technology specific and the value is stored in a MDIO register.

Module Low Power Pin :

Module Low Power Pin (MOD_LOPWR) is an input pin from the host, operating with active-high logic. It is pulled up in the CFP2. When MOD_LOPWR is asserted the CFP2 module is in the Low Power State and wil stay in the Low Power State as long as it is asserted. When de-asserted, the CFP2 initiates the Full-Power-up process. In Low Power mode the module can communicate via the MDIO management interface. While the module is in low power mode it has a maximum power consumption of <2W. This is protects hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Reset Pin:

Module Reset Pin (MOD_RSTn) is an input pin from the Host, operating with active-low logic. This pin is pulled down in the CFP2 with a pull-down resistor value of 4.7Kohm to 10Kohm.When MOD_RSTn is asserted (driven low) the CFP2 module enters the Reset State. When de-asserted, the CFP2 module comes out of the Reset State and shall begin an initialization process as part of the overall module startup sequence.

Programmable Alarm 1 Pin:

Programmable Alarm 1 Pin (PRG_ALRM1) is an output pin to the Host, operating with programmable logic. It can be re-programmed over MDIO registers to another MDIO alarm register while the module is in any steady state except Reset. MSA specifies the default function to be High Power On (HIPWR_ON) indicator with active-high logic.

The CFP2 MSA is designating that there be an intermediate state between the Low-Power state to the Module-Ready state, the TX-Off state. This state and default alarm function provides a defined state and signal where the CFP2 module is asserting wavelength control mechanisms and other high power funcitons. This default

function signals the host system that the CFP2 module is now ready for the transmitter to be enabled.

Programmable Alarm 2 Pin:

Programmable Alarm 2 Pin (PRG_ALRM2) is an output pin to the Host, operating with programmable logic. It can be re-programmed over MDIO registers to another MDIO alarm register while the module is in any steady state except Reset. MSA specifies the default function to be Module Ready (MOD_READY) indicator with active-high logic.

The default function MOD_READY is used by the CFP2 MSA during the module initialization. When asserted it indicates that the module has completed the necessary initialization process and is ready to transmit and receive data.

Programmable Alarm 3 Pin:

Programmable Alarm 3 Pin (PRG_ALRM3) is an output pin to the Host, operating with programmable logic. It can be re-programmed over MDIO registers to another MDIO alarm register while the module is in any steady state except Reset. MSA specifies the default function to be Module Fault (MOD_FAULT) indicator with active-high logic.

The default function MOD_FAULT is used by the CFP2 MSA during the module initialization. When asserted it indicates that the module has entered into a Fault state.

Module Absent Pin:

Module Absent Pin (MOD_ABS) is an output pin from CFP2 to Host. It is pulled up on the host board and is pulled down to groud in the CFP2 module. MOD_ABS asserts a Low condition when module is plugged in host slot. MOD_ABS is asserted High when the CFP2 module is physically absent from a host slot.

Receiver Loss of Signal Pin:

Receiver Loss of Signal Pin (RX_LOS) is an output pin to the Host, operating with active-high logic. When asserted, it indicates received optical power in the CFP2 module is lower than the expected value. The RX_LOS is the logic OR of the LOS signals from all the receiving channel in a CFP2 module.

Global Alarm Pin:

Global Alarm Pin (GLB_ALRMn) is an output pin to the Host, operating with active-low logic. When GLB_ALRMn is asserted (driven low), it indicates that a Fault/Alarm/Warning/Status (FAWS) condition has occurred. It is driven by the logical OR of all fault/status/alarm/warning conditions latched in the latched registers. Masking Registers are provided so that GLB_ALRMn may be programmed to assert only for specific fault/status/alarm/warning conditions. It is recommended that the Host board be designed to support a high

priority event handling service to respond to the assertion of this pin. Upon the assertion (driven low) of this pin, the Host event handler identifies the source of the fault by reading the latched registers over the MDIO interface. The reading action clears the latched register which in turn causes the CFP2 to de-assert (driven high) the GLB_ALRMn pin.

MDIO Pin:

The MDIO specification is defined in clause 45 of the IEEE 802.3 Standard. The CFP2 Module shall support 4.0 Mbit/s as maximum data rate. The CFP2 uses an MDIO with 1.2V LVCMOS logic levels.

MDC Pin:

Host specifies a maximum MDC rate of 4MHz and CFP2 module hence support a maximum MDC rate up to 4MHz. Other notable parameter is the minimal 10ns setup and hold time that the CFP2 module support in its MDIO implementation.

PRTADR0,1,2:

These control pins are used for the system to address all of the CFP2 ports contained within a host system. PRTADR0 corresponds to the LSB in the physical port addressing scheme. The 5-wire Physical Port Address lines are driven by host to set the module Physical Port Address which should match the address specified in the MDIO Frame. It is recommended that the Physical Port Address not be changed while the CFP2 module is powered on.

Pin Descriptions

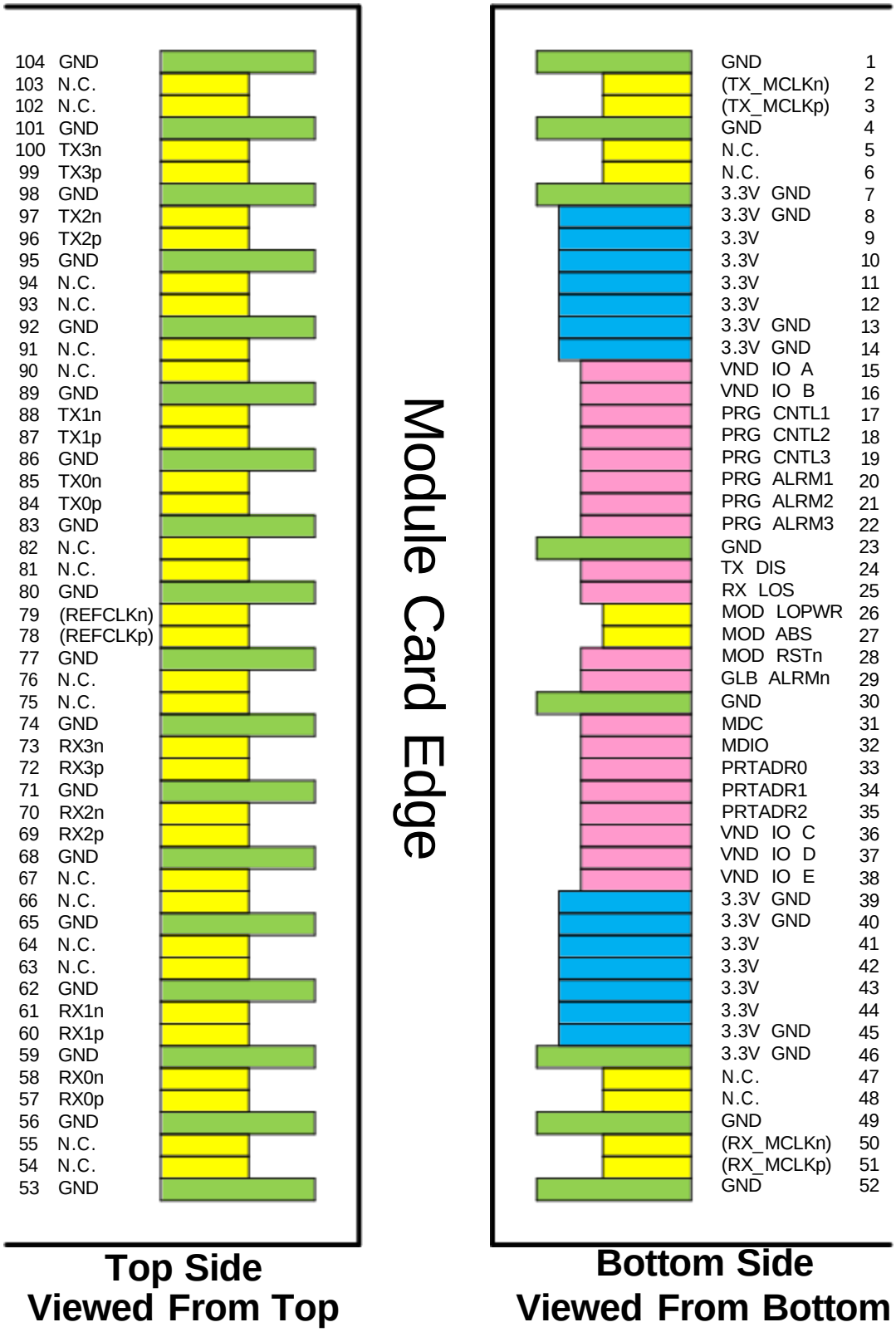

Figure 2. MSA compliant Connector

Pin	Symbol	Description	Notes
1	GND	Signal Ground	
2	(TX_MCLKn)	Not Supported	
3	(TX_MCLKp)	Not Supported	
4	GND	Signal Ground	
5	N.C.	No Connect	
6	N.C.	No Connect	
7	3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground	
8	3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground	
9	3.3V	3.3V Module Supply Voltage	
10	3.3V	3.3V Module Supply Voltage	
11	3.3V	3.3V Module Supply Voltage	
12	3.3V	3.3V Module Supply Voltage	
13	3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground	
14	3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground	
15	VND_IO_A	Module Vendor I/O A. Do Not Connect!	
16	VND_IO_B	Module Vendor I/O A. Do Not Connect!	
17	PRG_CNTL1	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used	
18	PRG_CNTL2	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤3W, "01": ≤6W, "10": ≤9W, "11" or NC: ≤12W = not used	
19	PRG_CNTL3	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤3W, "01": ≤6W, "10": ≤9W, "11" or NC: ≤12W = not used	
20	PRG_ALRM1	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0": module not high powered up	
21	PRG_ALRM2	Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, "1": Ready, "0": not Ready.	
22	PRG_ALRM3	Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault	
23	GND	Signal Ground	
24	TX_DIS	Transmitter Disable for all lanes, "1" or NC = transmitter disable, "0" = transmitter enabled	
25	RX_LOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition	
26	MOD_LOPWR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled	

27	MOD_ABS	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host	
28	MOD_RSTn	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module	
29	GLB_ALRMn	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host	
30	GND	Signal Ground	
31	MDC	Management Data Clock (electrical specs as per 802.3ae and ba). We recommends that the series matching resistor of MDC on host board should not be larger than 33ohm due to the voltage drop on the resistors may cause the logic high level mismatch. It is recommended that the host uses 1.3Kohm resistor to pull up the MDC. There is a 1Kohm pull-up resistor internally. The equivalent parallel pull-up resistance is 565ohm which is close to the optimized vaule (560ohm) specified in CFP MSA.	
32	MDIO	Management Data I/O bi-directional data (electrical specs as per IEEE 802.3-2012). We recommends that the series matching re-sistor of MDIO on host board should not be larger than 33ohm due to the voltage drop on the resistors may cause the logic high level mis-match. It is recommended that the host uses 1.3Kohm resistor to pull up the MDIO. There is a 1Kohm pull-up resistor internally. The equivalent parallel pull-up resistance is 565ohm which is close to the optimized vaule (560ohm) specified in CFP MSA.	
33	PRTADR0	MDIO Physical Port address bit 2	
34	PRTADR1	MDIO Physical Port address bit 1	
35	PRTADR2	MDIO Physical Port address bit 0	
36	VND_IO_C	Module Vendor I/O C. Do Not Connect!	
37	VND_IO_D	Module Vendor I/O D. Do Not Connect!	
38	VND_IO_E	Module Vendor I/O E. Do Not Connect!	
39	3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground	
40	3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground	
41	3.3V	3.3V Module Supply Voltage	
42	3.3V	3.3V Module Supply Voltage	
43	3.3V	3.3V Module Supply Voltage	
44	3.3V	3.3V Module Supply Voltage	
45	3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground	
46	3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground	
47	N.C.	For optical waveform testing. Not for normal use.	
48	N.C.	For optical waveform testing. Not for normal use.	

49	GND	Signal Ground	
50	(RX_MCLKn)	Not Supported	
51	(RX_MCLKp)	Not Supported	
52	GND	Signal Ground	
53	GND	Signal Ground	
54	N.C.	No Connect	
55	N.C.	No Connect	
56	GND	Signal Ground	
57	RX0p	Receiver ch0 data positive input. Internal AC coupled.	
58	RX0n	Receiver ch0 data negative input. Internal AC coupled.	
59	GND	Signal Ground	
60	RX1p	Receiver ch1 data positive output. Internal AC coupled.	
61	RX1n	Receiver ch1 data negative output. Internal AC coupled.	
62	GND	Signal Ground	
63	N.C.	No Connect	
64	N.C.	No Connect	
65	GND	Signal Ground	
66	N.C.	No Connect	
67	N.C.	No Connect	
68	GND	Signal Ground	
69	RX2p	Receiver ch2 data positive input. Internal AC coupled.	
70	RX2n	Receiver ch2 data negative input. Internal AC coupled.	
71	GND	Signal Ground	
72	RX3p	Receiver ch3 data positive input. Internal AC coupled.	
73	RX3n	Receiver ch3 data negative input. Internal AC coupled.	
74	GND	Signal Ground	
75	N.C.	No Connect	
76	N.C.	No Connect	
77	GND	Signal Ground	
78	(REFCLKn)	Not use, terminated internally	
79	(REFCLKp)	Not use, terminated internally	
80	GND	Signal Ground	
81	N.C.	No Connect	
82	N.C.	No Connect	
83	GND	Signal Ground	
84	TX0p	Transmitter ch0 data positive input. Internal AC coupled.	
85	TX0n	Transmitter ch0 data negative input. Internal AC coupled.	
86	GND	Signal Ground	
87	TX1p	Transmitter ch1 data positive input. Internal AC coupled.	
88	TX1n	Transmitter ch1 data negative input. Internal AC coupled.	
89	GND	Signal Ground	
90	N.C.	No Connect	
91	N.C.	No Connect	

92	GND	Signal Ground	
93	N.C.	No Connect	
94	N.C.	No Connect	
95	GND	Signal Ground	
96	TX2p	Transmitter ch2 data positive input. Internal AC coupled.	
97	TX2n	Transmitter ch2 data negative input. Internal AC coupled.	
98	GND	Signal Ground	
99	TX3p	Transmitter ch3 data positive input. Internal AC coupled.	
100	TX3n	Transmitter ch3 data negative input. Internal AC coupled.	
101	GND	Signal Ground	
102	N.C.	No Connect	
103	N.C.	No Connect	
104	GND	Signal Ground	

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Maximum Supply Voltage	Vcc	0	3.3	3.6	V	
Storage Temperature	Ts	-40		85	℃	
Relative Humidity	RH	15		85	%	1
Damage Threshold, each lane	THd	6.5			dBm	

Notes

1. Non-condensing

Operating Environments

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	3.2	3.3	3.4	V
Case Temperature	Top	0		70	℃
Link Distance with G.652				80	km

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power dissipation				12	W	
Supply Current	Icc			3.828	A	Steady state
CAUI-4 module input characteristics						
Signaling rate per lane (range)		25.78125±100ppm			Gbps	
Differential pk-pk input voltage tolerance	Vin,pp	900			mV	
Differential termination mismatch				10	%	
Eye width	EW15	0.46			UI	
Eye height	EH15	95			mV	
DC common mode voltage		-350		2850	mV	
CAUI-4 module output characteristics						
Signaling rate per lane (range)		25.78125±100ppm			Gbps	
AC common-mode output voltage	RMS			17.5	mV	
Differential output voltage	Vout,pp			900	mV	
Eye width	EW15	0.57			UI	
Eye height	EH15	228			mV	
Vertical eye closure	VEC			5.5	dB	
Differential termination mismatch				10	%	
Transition time	Tr/Tf	12			ps	20%~80%
DC common mode voltage		-350		2850	mV	

Optical Characteristics

100GBASE-ZR4 Operation（EOL, TOP = 0 to +70℃, VCC = 3.2 to 3.4 Volts）

Parameters	min	type	max	Unit	Note
Transmitter					
Signaling Speed per Lane	25.78125 ± 100 ppm			Gb/s	
Transmit wavelengths	1294.53		1296.59	nm	
	1299.02		1301.09		
	1303.54		1305.63		
	1308.09		1310.19		
Side-Mode Suppression Ratio (SMSR)	30			dB	
Total Average Launch Power	8.0		12.5	dBm	
Average launch power, each lane	2.0		6.5	dBm	
Average launch power of OFF transmitter, each lane			-30	dBm	
Extinction Ratio (ER)	6			dB	
RIN OMA			-130	dB/Hz	
Optical return loss tolerance			20	dB	
Transmitter reflectance			-12	dB	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Mask margin	5			%	1
Receiver					
Signaling Speed per Lane	25.78125 ± 100 ppm			Gb/s	
Receive wavelengths	1294.53		1296.59	nm	
	1299.02		1301.09		
	1303.54		1305.63		
	1308.09		1310.19		
Damage threshold	6.5			dBm	
Average receiver power, each lane	-28		-7	dBm	
Receiver Power, each lane(OMA)			-7	dBm	

Difference in receive power between any two lanes (Average and OMA)			3.5	dB	
Receiver reflectance			-26	dB	
Receiver sensitivity Average, each lane			-28	dBm	2
LOS Assert	-40			dBm	
LOS Deassert			-29	dBm	
LOS Hysteresis	0.5			dB	

Notes

1，Hit ratio 5×10^{-5}

2，Sensitivity is specified at BER@5E-5 with FEC

Digital Diagnostic Monitoring Functions

DDM accuracy requirements are defined as following table:

Performance Item	Monitor Error	Notes
Module temperature	+/-3°C	1，2
Module voltage	< 5%	2
LD Bias current	< 10%	2
Transmitter optical power	< 2dB	2
Receiver optical power	< 2dB	2

Note

1， Actual temperature test point is fixed on module case around Laser Array.

2， Full operating temperature range

Alarm and Warning Thresholds

It support alarms function, indicating the values of the preceding basic performance are lower or higher than the thresholds.

Performance Item	Low threshold	High threshold
Temp Alarm	-10 ℃	80 ℃
Temp Warning	0 ℃	70 ℃
Voltage Alarm	2.97 V	3.63 V
Voltage Warning	3.135 V	3.465 V
TX Power Alarm	-1 dBm	8.2 dBm
TX Power Warning	2 dBm	6.5 dBm
RX Power Alarm	-31 dBm	-4 dBm
RX Power Warning	-28 dBm	-7 dBm

Mechanical Specifications

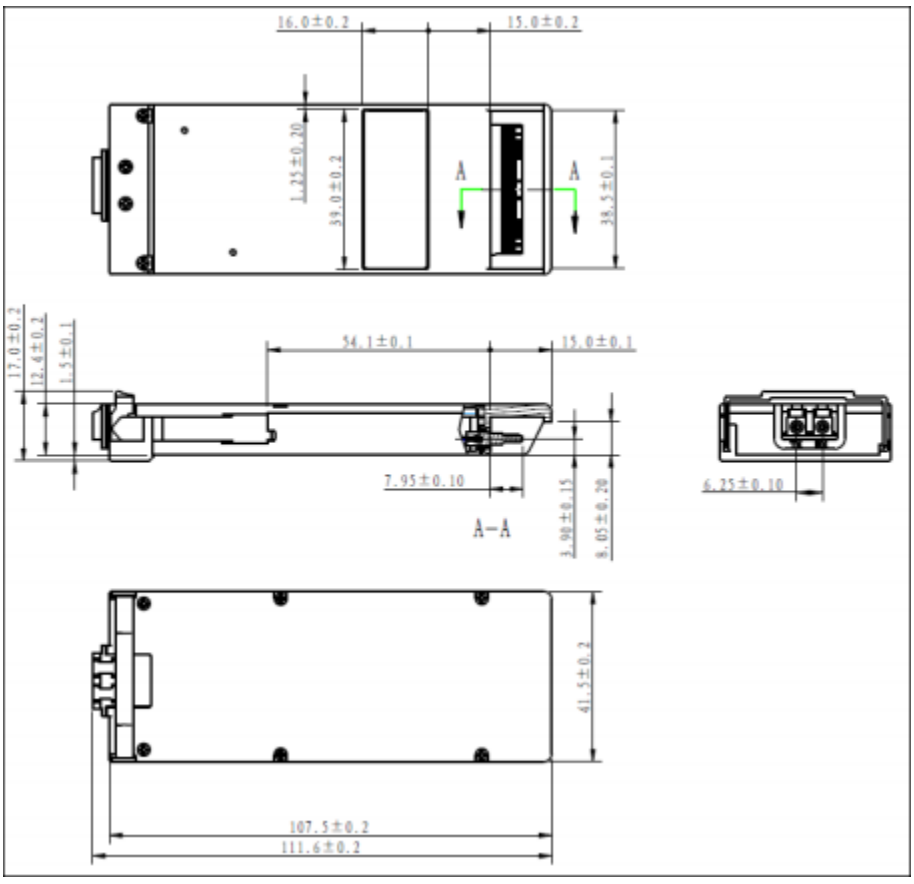

Figure 3. Mechanical Dimensions