Coherent 200G CFP2 DCO Module

Product Specification

Record of Version change：

Date	Version	Flag	Changes	Editor	Auditor	Approver
2020-02-07	V1.0	New	The specification of CFP2 DCO	Jacky		**Alex**

Note for column of Flag：

New – First writing of documents.

Add – The document is rewritten for the main purpose of adding new content.

Modify – The document is rewritten for the main purpose of modifying the error.

Upgrade – The whole document has been upgraded, designed to a larger change.

Contents

1. Introduction

This document describes the product specifications for coherent 200G CFP2 DCO modules based on dual polarization quadrature amplitude modulation (DP-16QAM) supporting extended C-band, polarization diversity coherent detection and advanced electronic link equalization. The module can accommodate various client signals such as 100/200 Giga-bit Ethernet (100GbE / 200GbE) and Optical Transport channel Uint-4(OUT4).The module will enable the following system performance and features:

1. Support Flex-grid channel spacing DWDM infrastructure

2. Support Flexible client-side interfaces:100GbE/200GbE, OTU4

3. Support OpenROADM(oFEC) line-side FEC types for 200G(31.57GBaud at DP-16QAM)

4. Framed PRBS generator/checker on the host and network side interfaces

5. Network and client loopback at the near-endian and far-endian point

6. CFP MSA IEEE802.3 Clause 45 compliant MDIO

7. Power consumption below 23W for 200G assuming

8. 104pin CFP2 MSA compliant connector

9. Hot Swappable

10. RoHS compliant

11. Compliant to OIF-CFP2-DCO-01.0, October 17, 2018

12. Compliant to CFP MSA Management Interface Specification, Version 2.6 r06a, March 27, 2017

1.1 Typical Application

The application field of the module is wide from short haul (ZR) to Metro (MR) and Data Center Interconnection (DCI). As shown in Figure 1, it is comprised of high-data lanes, a single 3.3V power supply, an MDIO interface for module control and status report, and dedicated alarm and control pins (not shown on the figure 1).
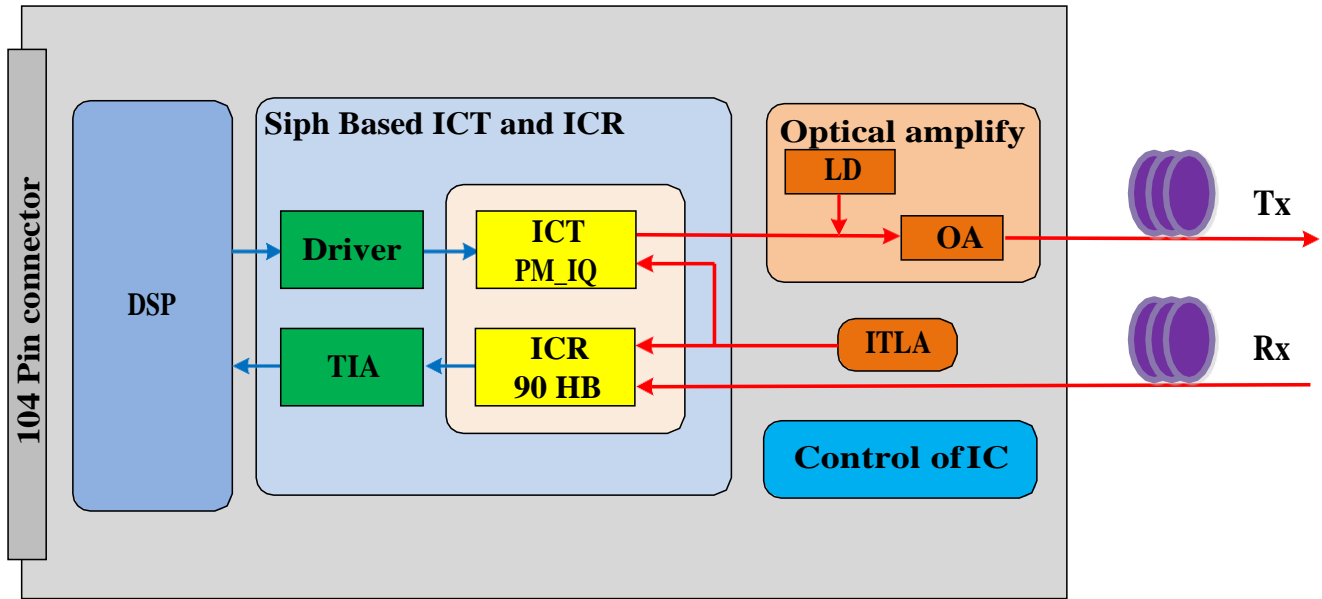
Figure 1:   Functional diagram of Module

1.2 Module Description

The Module uses a 104-pin OIF CFP2 Hardware Specification connector (Refer to OIF-CFP2-DCO-01.0.pdf) for all electrical interfaces with the host card, whereas the optical interfaces on the line side are provided throug h the optical receptacles on the CFP2. The module can be portioned into three functional parts: Tx path, Rx path and Control & Power block.

1.3 Path Description

The host interface is comprised of a total of 8 high-speed SerDes lanes. This allows module to support two interfaces for 200G application: an independent double 4-Lane mode client interfaces (for 2*100GbE, 2*OTU4 application), or a single 4-lane client interface (1* 200GbE application).

2. Module Configuration

The module is designed to maximize the number of use-cases in which it can be deployed. Both the host interface as well as the network interface can be configured for different applications.

2.1 Host Interface

The module supports many host signals types: table1 summarizes the supported client interface modes in the host interface. The electrical properties of the host interface are discussed in detail in section 3.

Table 1: Client interface

Client Side type	Client I/F mode	Client lane rate(Gb/s)	Note
1*200G	1*200GAUI-4	4*56Gbps(PAM4)	For 200G
2*100G	2*100CAUI-4	8*28Gbps(NRZ)	For 200G
2*OTU4	2*OTL4.4	8*28Gbps(NRZ)	For 200G

The host rate is dependent on the framing type and the supported host rates are shown in the following table.

Table 2: Host Rates

Host Frame	Host Data Bit Rate(Gbps)	Offset(ppm)	Singal
1*200G KP4	1*212.5	100	Ethernet class
2*100G	2*100G/106.25(KP4)/103.125(KR4)	100	Ethernet class
2*OTU4	2*111.8099736	20	

2.2 FEC mode

The information of FEC mode and modulation mode is as followed table.

Table 3: Line FEC Type and modulation mode

Id	Application	Modulation	FEC Type	Lane Baud	Grid	OSNR	Note
1	200G	DP-16QAM	oFEC	31.57G	50G	19.5	

3. Product Specifications

3.1 Absolute maximum ratings

The absolute maximum ratings given in the table below define the damage thresholds. Hence, the component shall withstand the given limits without any irreversible damage.

Table 4: Absolute Maximum Ratings

Item	Parameter	Condition [1]	Min	Max	Unit
1	Storage Temperature Range		-40	85	°C
2	Storage Humidity	Relative, no-Condensing	-	85	%
3	Case Temperature Range		-10	+70	°C
4	Power supply		-0.3	3.7	V
5	Input power(Optical)	Peak Power		10	dBm

Note: 1.Top=25℃, unless otherwise specified.

3.2 Operating conditions

Table 5: Operating Environment

Item	Parameter	Condition	Symbol	Min	Max	Unit
1	Operating Case Temperature (Top)		T_{case}	0	70	°C
2	Relative humidity Range	Non-condensing	RH	-	85	%
3	Operating Input Optical Power of Signal		P_{sig}	-18	+5	dBm
4	Storage Temperature Range			-40	85	°C

3.3 Electrical Specifications

3.3.1. Power supply

Table 6: Power specifications

Item	Parameter	Condition	Min	Type	Max	Unit
1	3.3V DC Power Supply Voltage		3.2	3.3	3.4	V
2	3.3V DC Power Supply Current				8	A
3	Power Consumption	Low Power			2	W
4	Power Consumption @ DP-16QAM with oFEC for 200G			22		W
5	Inrush current	Power class 5 & 6			300	mA/us
6	Turn-off current	Power class 5 & 6	-300			mA/us
7	Power Supply Noise	DC - 1MHz			2	%
8	Power Supply Noise	1 - 10MHz			3	%

3.3.2. Hardware Control Pins

The control and status reporting functions between a host and a CFP2 module use non-data control and status reporting pins on the 104-pin connector. The control and status reporting pins work together with the MDIO interface to form a complete HOST-CFP2 management interface. The status reporting pins provide status reporting. There are six (6) Hardware Control pins, five (5) Hardware Alarm pins, and six (6) pins dedicated to the MDIO interface. Specification of the CFP2 hardware signaling pins are given in Ref. [1] with the following changes listed in this section. The module supports real-time control functions via hardware pins, listed in table 7 as bellow.

Table 7: Control Pins

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
17	PRG_CNTL1	Programmable Control 1 *MSA Default: TRXIC_RSTn, TX & RX ICs reset,* *"0": reset, "1"or NC: enabled*	I	3.3V LVCMOS	per CFP MSA MIS Ref. [7]		Pull – Up[2]
18	PRG_CNTL2	Programmable Control 2 *MSA Default: Hardware Interlock LSB*	I	3.3V LVCMOS			Pull – Up[2]
19	PRG_CNTL3	Programmable Control 3 *MSA Default: Hardware Interlock MSB*	I	3.3V LVCMOS			Pull – Up[2]
24	TX_DIS	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull – Up[2]
26	MOD_LOPWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull – Up[2]
28	MOD_RSTn	Module Reset, Active Low (invert)	I	3.3V LVCMOS	Enable	Reset	Pull – Down[3]

[2]Pull-Up resistor (4.7 kOhm to 10 kOhm) is located within the CFP2 module

[3]Pull-Down resistor (4.7 kOhm to 10 kOhm) is located within the CFP2 module

3.3.3. Hardware Alarm Pins

The CFP2 Module supports alarm hardware pins as listed in Table 8.

Table 8: Alarm Pins

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
20	PRG_ALRM1	Programmable Alarm 1 *MSA Default: HIPWR_ON*	O	3.3V LVCMOS			
21	PRG_ALRM2	Programmable Alarm 2 *MSA Default: MOD_READY, Ready state has been reached*	O	3.3V LVCMOS	Active High per CFP MSA MIS Ref. [7]		
22	PRG_ALRM3	Programmable Alarm 3 *MSA Default: MOD_FAULT*	O	3.3V LVCMOS			
25	RX_LOS	Receiver Loss of Signal	O	3.3V LVCMOS	Loss of Signal	OK	
27	MOD_ABS	Module Absent	O	3.3V LVCMOS	Absent	Present	Pull Down[2]

3.3.4. Management Interface Pins

The CFP2 Module supports alarm, control and monitor functions via an MDIO bus. Upon module initialization, these functions are available. CFP2 MDIO electrical interface consists of six (6) pins including two (2) pins for MDC and MDIO, three (3) Physical Port Address pins, and the Global Alarm pin.
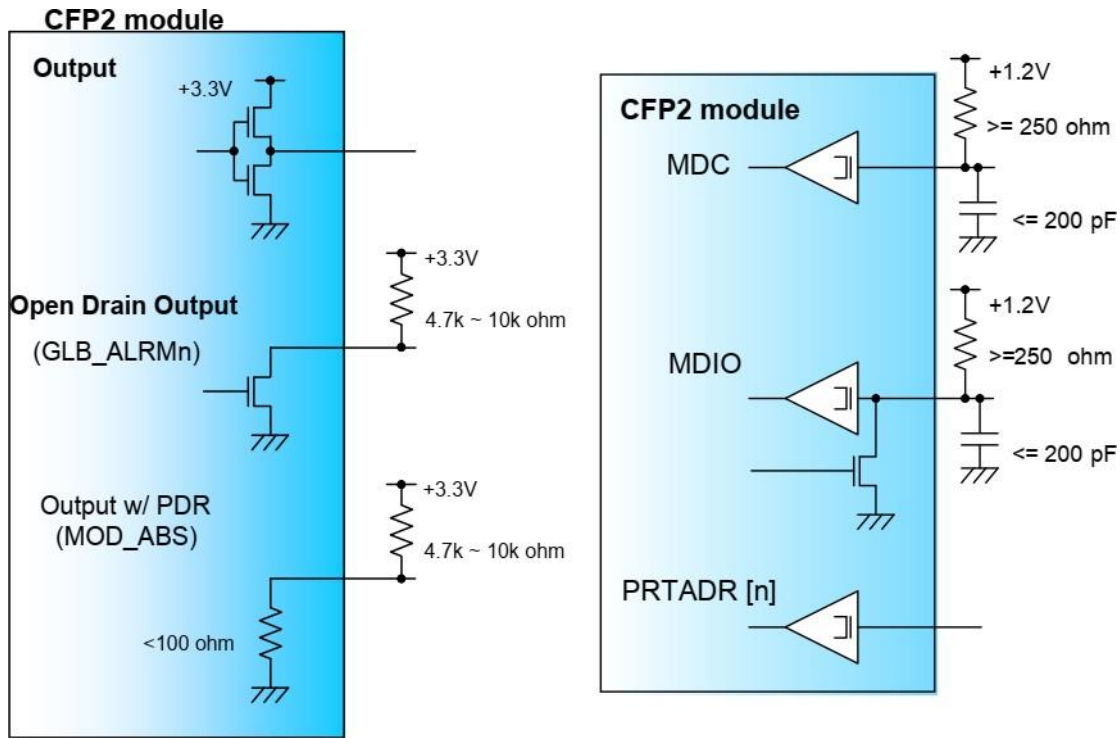
Figure 2: **Reference +3.3V LVCMOS Output and MDIO Interface Termination**

MDC is the MDIO Clock line driven by the host and MDIO is the bidirectional data line driven by both the host and module depending upon the data directions. The CFP2 MDIO pins are listed in Table 9.

Table 9: Management Interface Pins (MDIO/MDC)

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
29	GLB_ALRMn	Global Alarm	O	3.3V LVCMOS	OK	Alarm	
31	MDC	MDIO Clock	I	1.2V LVCMOS			
32	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS			
33	PRTADR0	MDIO Physical Port address bit 0	I	1.2V LVCMOS	per CFP MSA MIS Ref. [7]		
34	PRTADR1	MDIO Physical Port address bit 1	I	1.2V LVCMOS			
35	PRTADR2	MDIO Physical Port address bit 2	I	1.2V LVCMOS			

3.3.5. Module Management Interface Description

The CFP2 module utilizes MDIO IEEE Std 802.3TM-2012 clause 45 for its management interface. The CFP2 MDIO implementation is defined in a separate document entitled, "OIF-CFP2-DCO-01.0, Revision 1.0, October 17, 2018". When multiple CFP2 modules are connected via a single bus, a particular CFP2 module can be selected by using the Physical Port Address pins.

3.4 High-Speed Electrical Specifications

The transmitter and receiver comply with the CEI-56G-VSR-PAM4 or CEI-28G-VSR electrical specification (OIF-CEI-04.0). The data lines are AC-coupled and terminated in the module per the following figure from the CFP2 MSA.

The Module high speed electrical interface supports the following configurations:

1) 4 tx lanes + 4 rx lanes, each at 56Gbit/s

2) 8 tx lanes + 8 rx lanes, each at 28Gbit/s

3.4.1. Loopback

The module support loopback functionality. The host loopback (Loopback 1: As be shown on figure3) and the network loopback (Loopback 2: As be shown on figure5) are oriented per Figure 7 shown below. For details on controlling the loopback mode, please refer to Reference [1]. In optional loopback, TXn is looped back to RXn, for example TX0+ to RX0+, on both host and network side.
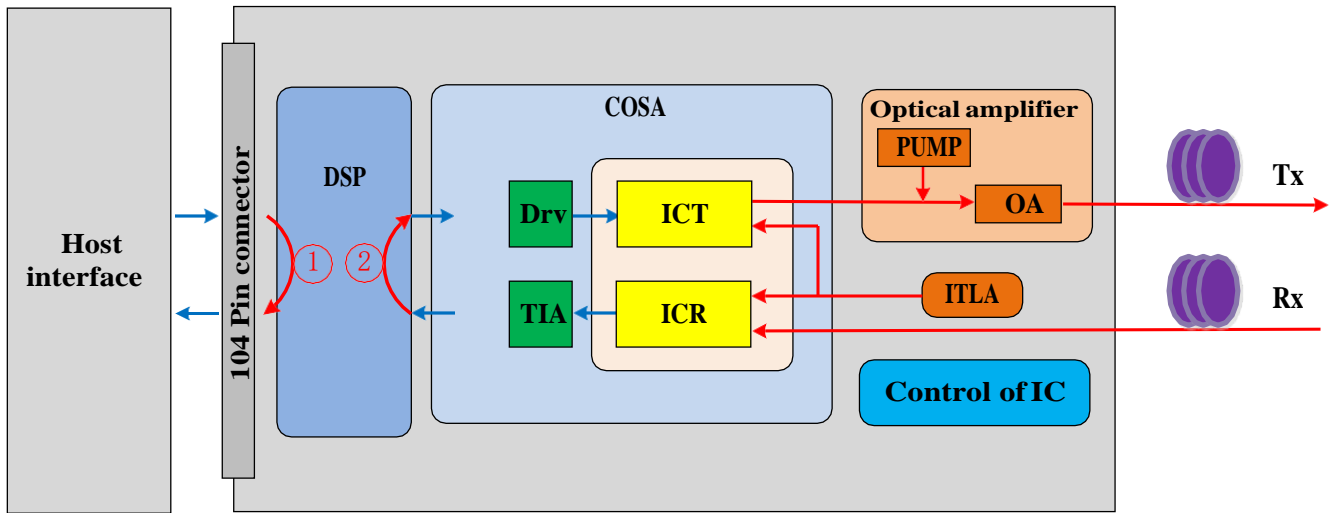

Figure 3:   Module Loopback Orientation

3.4.2. Reference Clock

There has local reference clock in this module, so the module don't need the external 1/160 or 1/32 reference clock which is came from the pin 78 and pin 79, the pins can be in disconnected status.

3.5 Optical Specifications

Unless noted all specifications given in this document are End-of-Life numbers and are valid over case temperature from 0°C to +70°C.

3.5.1. Optical Transmitter Specifications

There are show all Transmitter specifications in the bellow table 10.

Table 10:   Optical Transmitter Specifications

Id	Parameter	Type	Min	Max	Unit	Condition/comments
1	Transmitter Frequency Range		191.3	196.10	THz	C band 50GHz ITU-T grid. Frequency range over which the specifications hold unless noted otherwise.
2	Channel Spacing	50			GHz	
3	Frequency Stability		-1.8	1.8	GHz	Frequency stability relative to ITU grid.
4	Frequency Offset		-1.8	1.8	GHz	
5	Frequency Fine Tuning Range		-6.0	6.0	GHz	
6	Fine Tuning Resolution	100			MHz	
7	Fine Tuning Time			6	s	
8	Channel Tuning Speed			30	s	
9	Line Width		100	300	kHz	FWHM
10	SMSR (Side mode suppression Ratio)	45	40		dB	Measured over +/-2.5nm range around the target frequency with 0.06nm RBW without modulation.
11	Transmitter output power range		-10	+2	dBm	Transmitter output is settable in steps of 0.1 dB at any power level within the specified frequency range
12	Output power stability		-0.5	0.5	dB	Output power change over temperature and over time, measured over 10ms second intervals.
13	Output power stability(BOL)		-0.5	0.5	dB	Difference over temperature, time, wavelength and aging.
14	Output power accuracy(EOL)		-1	1	dB	Difference between the set value and actual value over aging.
15	Transmitter turn-up time from warm start		-	100	ms	Module is in Ready state. The maximum transmitter turn-up time is counted from de-assert the Tx_disable Pin to full Tx turn-up.
16	Transmitter laser disable time		-	100	ms	Tx is in full turn-up state. The maximum transmitter turn-off time is counted from assert Tx_disable pin
17	Transmitter turn-up time from cold start		-	90	s	Module is in Low_Power mode. The maximum Tx turn-up time is counted from de-assert the Low_power pin and Tx_disable pin to full Tx turn-up.
18	Transmitter OSNR		38		dB/0.1nm	OSNR at transmitter output (in-band)
19	Transmit signal-to-max ASE		35		dB/0.1nm	Signal to the maximum out-of-band ASE level
20	Transmitter optical return loss		27	-	dB	
21	Transmitter output power with TX disabled			-40	dBm	
22	Transmitter polarization dependent power			1	dB	Power deference between X and Y polarization

3.5.2. Optical Receiver Specifications

Table 11 contains the general receiver specifications for 200G DP-QPSK oFEC.

Table 11:   Optical Receiver Specifications with DP-16QAM at oFEC for 200G

Id	parameter	Type	Min	Max	Unit	Condition/comments
1	Receiver Frequency Range		191.3	196.10	THz	C band 50GHz ITU-T grid.
2	Input power range		-18	+5	dBm	Signal power of the selected channel
3	Receiver Sensitivity			-24	dBm	Minimum input power needed to achieve post FEC BER < 10-15 when OSNR > 35dB and internal FEC enabled
4	OSNR Sensitivity	19.5			dB/0.1nm	At internal FEC threshold (post FEC BER < 10-15), at optimum Input power as specified above.
5	Los assert		-22		dBm	
6	Los de-assert			-20	dBm	
7	Los hysteresis			2	dB	
8	CD Tolerance			160	ns/nm	with less than 0.5dB OSNR penalty at FEC.
9	DGD tolerance		150		ps	
10	PDL tolerance		3		dB	See note 2 for detail information.
11	Tolerance to change in SOP		200	-	rad/ms	Tolerance to change in SOP with OSNR sensitivity specs at FEC threshold.(16KHz)
12	Input power transient tolerance		5	-	dB	See note 3 for detail information.
13	Dispersion reading accuracy		-3%	3%	ps/nm	The receiver reports the amount of dispersion being compensated.
14	DGD reading accuracy		-4	4	ps	The receiver reports the amount of DGD being compensated.
15	Input power reading accuracy		-1	1	dB	The module reports the actual power as received by the module.
16	Optical Return Loss		27		dB	
17	Receiver turn-up time from cold start		-	90	Seconds	Module is in Low_power state and valid Rx input signal is ready. The time from de-assert Low_power pin to full Rx turn-up, given that valid line side signal is ready.

4. Mechanical Specifications

4.1. Mechanical Overview & Dimensions

The CFP2 module is 107.5x41.5x12.4mm in size and is mechanically compliant to the requirements detailed the CFP2 Hardware Specification rev. 1.0.   The module is designed to be inserted into a host board with a railing system that includes a heat sink.
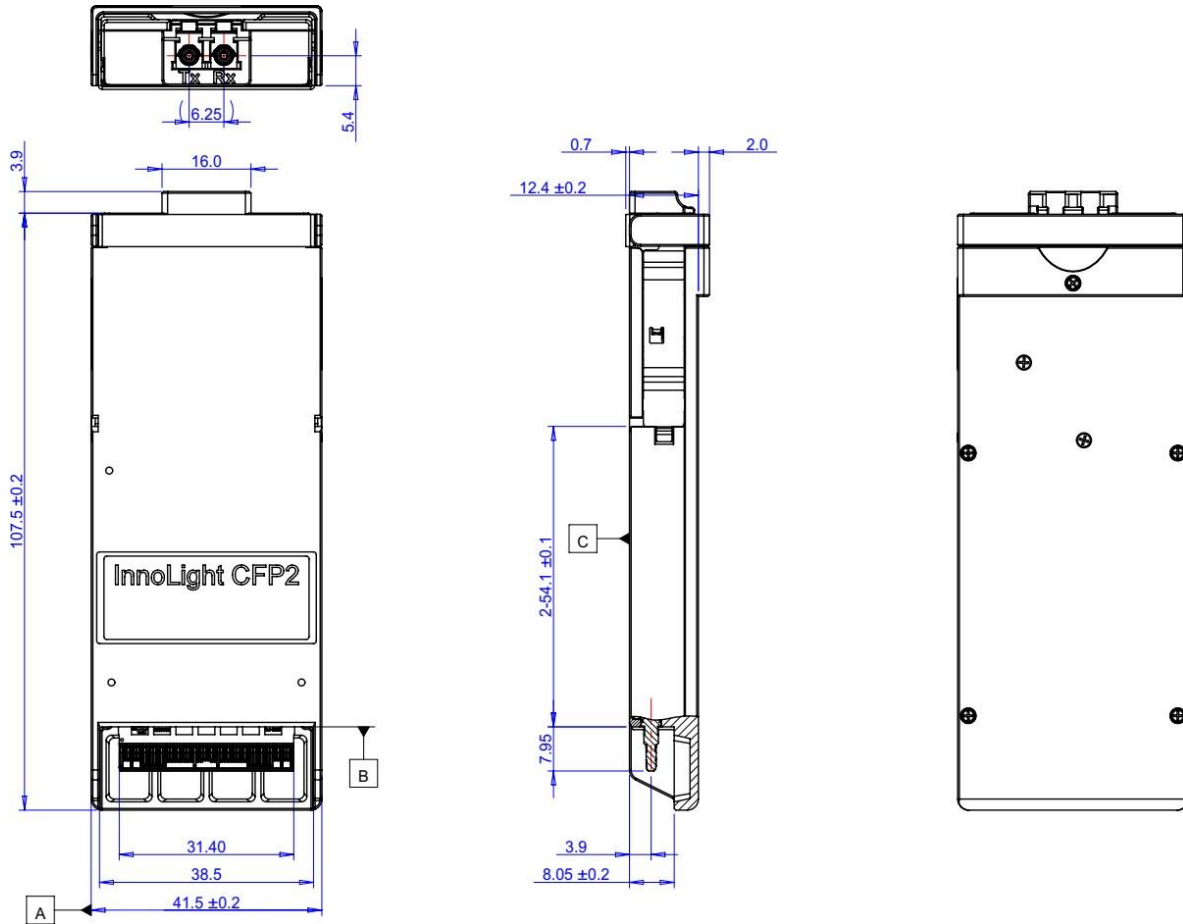
Figure 4:   Mechanical Overview for CFP2

4.2.　Host Electrical Connector & Pin Assignments

The module plug connector is a sub-component within the CFP2 module. The PCB inserts into the connector with a top and bottom row of pins (primary and secondary side PCB). The host connector has a physical offset of the pin contacts to ensure certain signals make and break contact before others. Ground mates first, the 3.3V and 3.3V ground mate second, the control and status signals mate third, and the MOD_LOPWR, MOD_ABS and high-speed data signals mate last. The module connector is a 104-pin plug connector and the connector pinout defined by the OIF-CFP2-DCO-01.0. All pins are showed as figure 5.

4.2.1. CFP2 Pin-Map

Pin Number	Name of Pin		Pin Number	Name of Pin
1	GND		104	GND
2	OHIO_RDn		103	TX4n
3	OHIO_RDp		102	TX4p
4	GND		101	GND
5	OHIO_TDn		100	TX3n
6	OHIO_TDp		99	TX3p
7	3.3V GND		98	GND
8	3.3V GND		97	TX2n
9	3.3V		96	TX2p
10	3.3V		95	GND
11	3.3V		94	TX5n
12	3.3V		93	TX5p
13	3.3V GND		92	GND
14	3.3V GND		91	TX6n
15	VND_IO_A		90	TX6p
16	VND_IO_B		89	GND
17	PRG_CNTL1		88	TX1n
18	PRG_CNTL2		87	TX1p
19	PRG_CNTL3		86	GND
20	PRG_ALRM1		85	TX0n
21	PRG_ALRM2		84	TX0p
22	PRG_ALRM3		83	GND
23	GND		82	TX7n
24	TX_DIS		81	TX7p
25	RX_LOS		80	GND
26	MOD_LOPWR		79	(REFCLKn)
27	MOD_ABS		78	(REFCLKp)
28	MOD_RSTn		77	GND
29	GLB_ALRMn		76	RX4n
30	GND		75	RX4p
31	MDC		74	GND
32	MDIO		73	RX3n
33	PRTADR0		72	RX3p
34	PRTADR1		71	GND
35	PRTADR2		70	RX2n
36	VND_IO_C		69	RX2p
37	VND_IO_D		68	GND
38	VND_IO_E		67	RX5n
39	3.3V GND		66	RX5p
40	3.3V GND		65	GND
41	3.3V		64	RX6n
42	3.3V		63	RX6p
43	3.3V		62	GND
44	3.3V		61	RX1n
45	3.3V GND		60	RX1p
46	3.3V GND		59	GND
47	OHIO_REFCLKn		58	RX0n
48	OHIO_REFCLKp		57	RX0p
49	GND		56	GND
50	Reserved		55	RX7n
51	Reserved		54	RX7p
52	GND		53	GND

Figure 5:   CFP2 4*56G or 8*28G bit/s pin-map

The bottom pins of module are described as followed table.

Table 12:   The description of Bottom pin

Pin Number	Name of Pin	Structure (Input/Output)	Logic	Description / Connection
1	GND	GND	Ground	
2	OHIO_RDn	O	CML	OHIO output
3	OHIO_RDp	O	CML	OHIO output
4	GND	GND	Ground	
5	OHIO_TDn	I	CML	OHIO input
6	OHIO_TDp	I	CML	OHIO input
7	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
8	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
9	3.3V	PWR	Power	3.3V Module Supply Voltage
10	3.3V	PWR	Power	3.3V Module Supply Voltage
11	3.3V	PWR	Power	3.3V Module Supply Voltage
12	3.3V	PWR	Power	3.3V Module Supply Voltage
13	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
14	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
15	VND_IO_A	I/O	N.C	Module Vendor I/O A. Do Not Connect!
16	VND_IO_B	I/O	N.C	Module Vendor I/O B. Do Not Connect!
17	PRG_CNTL1	I	LVCMOS w/PUR	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled
18	PRG_CNTL2	I	LVCMOS w/PUR	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤9W, "01": ≤12W, "10": ≤15W, "11" or NC:
19	PRG_CNTL3	I	LVCMOS w/PUR	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤9W, "01": ≤12W, "10": ≤15W, "11" or NC:
20	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1; MSA Default "H" = HIPWR_ON
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2; MSA Default "H" = MOD_READY
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3; MSA Default "H" = MOD_FAULT
23	GND	GND	Ground	
24	TX_DIS	I	LVCMOS w/PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
26	MOD_LOPWR	I	LVCMOS w/PUR	Module Low Power Mode. "1" or NC: module in low power (safe)
27	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
28	MOD_RSTn	I	LVCMOS w/PUR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module

29	GLB_ALRMn	O	LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up
30	GND	GND	Ground	
31	MDC	I	1.2V LVCMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)
32	MDIO	I/O	1.2V LVCMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3-2012)
33	PRTADR0	I	1.2V LVCMOS	MDIO Physical Port Address bit 0
34	PRTADR1	I	1.2V LVCMOS	MDIO Physical Port Address bit 1
35	PRTADR2	I	1.2V LVCMOS	MDIO Physical Port Address bit 2
36	VND_IO_C	I/O	N.C	Module Vendor I/O C. Do Not Connect!
37	VND_IO_D	O	1.8C LVCMOS	Module Vendor I/O D. Do Not Connect!
38	VND_IO_E	I/O	N.C	Module Vendor I/O E. Do Not Connect!
39	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply return path.
40	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply return path.
41	3.3V	PWR	Power	3.3V power supply
42	3.3V	PWR	Power	3.3V power supply
43	3.3V	PWR	Power	3.3V power supply
44	3.3V	PWR	Power	3.3V power supply
45	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply return path.
46	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply return path.
47	OHIO_REFCLKn	I	CML	OHIO ref clk input
48	OHIO_REFCLKp	I	CML	OHIO ref clk input
49	GND	GND	Ground	Module Ground. Logic and power return path
50	Reserved	O	CML	For optical waveform testing or Module vendor output
51	Reserved	O	CML	For optical waveform testing or Module vendor output
52	GND	GND	Ground	Module Ground. Logic and power return path

Table 13:   The description of Top pin

	4x28G NRZ	8x28G NRZ	2x56G PAM4	4x56G PAM4	Description
	Name				
104	GND	GND	GND	GND	Ground
103	N.C.	TX4n	N.C.	N.C.	Transmitter lane 4 / N.C
102	N.C.	TX4p	N.C.	N.C.	
101	GND	GND	GND	GND	Ground
100	TX3n	TX3n	N.C.	TX3n	Transmitter lane 3 / N.C
99	TX3p	TX3p	N.C.	TX3p	
98	GND	GND	GND	GND	Ground
97	TX2n	TX2n	N.C.	TX2n	Transmitter lane 2 / N.C
96	TX2p	TX2p	N.C.	TX2p	
95	GND	GND	GND	GND	Ground
94	N.C.	TX5n	N.C.	N.C.	Transmitter lane 5 / N.C
93	N.C.	TX5p	N.C.	N.C.	
92	GND	GND	GND	GND	Ground
91	N.C.	TX6n	N.C.	N.C.	Transmitter lane 6 / N.C
90	N.C.	TX6p	N.C.	N.C.	
89	GND	GND	GND	GND	Ground
88	TX1n	TX1n	TX1n	TX1n	Transmitter lane 1
87	TX1p	TX1p	TX1p	TX1p	
86	GND	GND	GND	GND	Ground
85	TX0n	TX0n	TX0n	TX0n	Transmitter lane 0
84	TX0p	TX0p	TX0p	TX0p	
83	GND	GND	GND	GND	Ground
82	N.C.	TX7n	N.C.	N.C.	Transmitter lane 7 / N.C
81	N.C.	TX7p	N.C.	N.C.	
80	GND	GND	GND	GND	Ground
79	(REFCLKn)	(REFCLKn)	(REFCLKn)	(REFCLKn)	N.C
78	(REFCLKp)	(REFCLKp)	(REFCLKp)	(REFCLKp)	
77	GND	GND	GND	GND	Ground
76	N.C.	RX4n	N.C.	N.C.	Receiver lane 4 / N.C
75	N.C.	RX4p	N.C.	N.C.	
74	GND	GND	GND	GND	Ground
73	RX3n	RX3n	N.C.	RX3n	

72	RX3p	RX3p	N.C.	RX3p	Receiver lane 3 / N.C
71	GND	GND	GND	GND	Ground
70	RX2n	RX2n	N.C.	RX2n	Receiver lane 2 / N.C
69	RX2p	RX2p	N.C.	RX2p	
68	GND	GND	GND	GND	Ground
67	N.C.	RX5n	N.C.	N.C.	Receiver lane 5 / N.C
66	N.C.	RX5p	N.C.	N.C.	
65	GND	GND	GND	GND	Ground
64	N.C.	RX6n	N.C.	N.C.	Receiver lane 6 / N.C
63	N.C.	RX6p	N.C.	N.C.	
62	GND	GND	GND	GND	Ground
61	RX1n	RX1n	RX1n	RX1n	Receiver lane 1
60	RX1p	RX1p	RX1p	RX1p	
59	GND	GND	GND	GND	Ground
58	RX0n	RX0n	RX0n	RX0n	Receiver lane 0
57	RX0p	RX0p	RX0p	RX0p	
56	GND	GND	GND	GND	Ground
55	N.C.	RX7n	N.C.	N.C.	Receiver lane 7
54	N.C.	RX7p	N.C.	N.C.	
53	GND	GND	GND	GND	Ground

4.2.2. The differents of High-speed Pin-Map for 100G/200G application

For 200G application, there are two interface modes: 8*28G NRZ or 4*56G PAM4, which can be supported: 2*100CAUI-4/100GAUI-2, 2* OTL4.4 /OTL4.2 or 1*200GAUI-4.

Table 14:   The pin-map of High-speed pin for 100G/200G application

SerDes Lanes	200G		
	200GAUI-4 (PAM4)	2*CAUI-4 2*OTL4.4 (NRZ)	2*100GAUI-2 2*OTL4.2 (PAM4)
	Interface - CH[x,y]		
Tx7[p,n];Rx7[p,n]	NC	CH2.2	NC
Tx6[p,n];Rx6[p,n]			
Tx5[p,n];Rx5[p,n]			
Tx4[p,n];Rx4[p,n]			
Tx3[p,n];Rx3[p,n]	CH2.1	CH2.1	CH2.2
Tx2[p,n];Rx2[p,n]			
Tx1[p,n];Rx1[p,n]			CH2.1
Tx0[p,n];Rx0[p,n]			
Note: 1. The CFP2 Host/Client interface naming convention is CH, where, CH=Channel, 2. <x>.<y>: <x> = channel capacity, where [x=1,2] is 1=100G or 2=200G. <y> = channel numeration, where [y=1 …3] is channel numeration. 3.NC – No connected			

5. ESD

This transceiver is specified as ESD threshold 250V for according to GR-78 (Human Body Model using C= 100pF, R = 1.5kOhm) on the high speed pins and 500v for all others electrical pins. However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

6. Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

7. Order Information

The part number of coherent module is as described as followed table 15.

Table 15:   Rules of part number

CT	-	XX	X	XXX	X	XX	X	X	XX
Note1		Form Factor: QD: QSFP-DD OS: OSFP CP: CFP CT: CFP2 MA: MSA	Number of Channels: S: 1 Ch D: 2 Ch	Data Rate (Single Channel): 100: 100 Gbit/s 200: 200 Gbit/s 300: 300 Gbit/s 400: 400 Gbit/s 600: 600 Gbit/s 800: 800 Gbit/s	Rate Select: S: Single Rate D: Dual Rate T: Triple Rate M: Multi-Rate (supports four rates and above)	Transmission Distance: ER: 10~40km ZR: ZR(~100km) MR: MR(~1000km) LH: LR(~2000km) UH: ULH(>2000km)	Wavelength: F:Fixed Wavelength; T:C-band Tunable Wavelength;	Temperature Range: N: -5 to 70℃ A: 0 to 70℃ E: -10 to 70℃	Customer Code: 00: Standard BK: Blank CI: Cisco

Note: 1. **CT - Coherent Transceiver**

For examples:

1)   CT-CTS200SMRTA00: Single rate 200Gb/s single channel tunable coherent CFP2 MR, 0 ~ 70℃;

8. Glossary

Table 16:   Glossary

Glossary	Info.
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
BS	Beam Splitter
CMRR	Common Mode Rejection Ratio
DSP	Digital Signal Processor
IA	Implementation Agreement
LO	Local Oscillator
MGC	Manual Gain Control
MPD	Monitor Photodiode
MSA	Multi-Source Agreement
OIF	Optical Internetworking Forum
PBS	Polarization Beam Splitter
PCB	Printed Circuit Board
PM-QPSK	Polarization Multiplexed Quadrature Phase Shift Keying
DP-QPSK	Dual Polarization Quadrature Phase Shift Keying
DP-16QAM	Dual Polarization Quadrature Amplitude Modulation
PCS-16QAM	Probabilistic Constellation Shaping Quadrature Amplitude Modulation
OUT4	Optical Transport channel Uint-4
OTUCn	Optical Transport Unit Cn

9. Reference Documents

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IEEE Std 802.3TM-2012, Cl. 45, Management Data Input/output (MDIO) Interface. [9].

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[13]. GFEC: ITU-T G.709 standard FEC

[14]. SCFEC: Staircase FEC -- ITU-T G.709.2(07/2018)

[15]. KR4-FEC: KR4-FEC for 100GbE Client RS(528, 514) -- IEEE802.3 standard Refer to Clause 74, 91

[16]. KP4-FEC: KP4-FEC for 100GbE/200GbE/400GbE Client RS(544, 514) -- IEEE802.3 standard Refer to Clause 91, 119

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